THE EFFECTS OF NONUNIFORMITY ON THE MODELING OF RESISTIVITY IN POLYCRYSTALLINE SILICON THIN FILMS

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This research is concerned the electrical and transport properties in the Low Pressure Chemical Vapor Deposited (LPCVD) polycrystalline silicon thin film resistors. There are currently many uses of polysilicon in the integrated circuit industry, but these uses are constrained by the lack of control over the electrical properties of this material. This problem is a direct result of the nonuniformity in the physical nature of this material. Current models of the electronic properties involve detailed analysis of the abstract conduction mechanisms while ignoring the more realistic aspects of the observed characteristics. This research attempts to provide a new theory of practical use for the modelling of the characteristics of this material. The theory developed by this study explicitly models the nonuniform characteristics by the use of distribution functions. The model is also applied to characterize the experimental results of the electrical properties of variously processed LPCVD polysilicon. The study also develops a procedure for the determination of the location of the charge subsets by extraction from experimental results. Included in the study ia an investigation of the microstructure by Transmission Electron Microscope.

The theory developed by this investigation is applied to the evaluation of the resistivity function of temperature for polycrystalline silicon thinfilm material. The derived function includes the effects of the variation in grain boundary barrier heights, the grain boundary surface to volume ratio, a carrier density which is constant with temperature and the thermionic emission conduction mechanism. Also, the calculation of the amount of charge trapped at the grain boundaries is modified to include the effect of a dopant profile near the grain boundary. All parameters in the model are constants with temperature and are determined from experiment.

CHAPTER I

INTRODUCTION

Polycrystalline silicon (polysilicon) is rapidly becoming a very important material in integrated circuit fabrication. Thin film polysilicon produced by Low Pressure Chemical Vapor Deposition (LPCVD) is now used for poly-gates, interconnects, resistors, passivation and contacting, especially in the new self-aligned processes. As applications proliferate, better understanding of the electronic process of conduction is essential. This material has been studied for many years, and the basic electrical properties have been determined to be unique to polysilicon [1,2,3,4]. This research has provided the basis for the two dominant theories for conduction in polysilicon, the grain boundary trapping theory [5,6] and the dopant segregation theory [4,7]. These theories provide models of the conduction mechanisms, but cannot accurately predict all the observed characteristics. To be practically useful, it is important for a model to have the the ability to predict the electronic characteristics of polysilicons prepared from varying processes, but this is not possible with current models. The modeling of polysilicon is very difficult due to the complex mechanisms involved, and relies on many simplifying assumptions. Special problems develop when modeling temperature variation, since this must involve the explicit physical mechanisms [8,9,10].

Current models often involve the use of several somewhat arbitrary parameters, where physical variables such as grain size or boundary width are allowed to vary with temperature. This project will develop a modified theoretical model, and apply it to characterize the resistivity versus temperature characteristic for the LPCVD polysilicon thin films prepared under various implant and annealing conditions. No parameters will be allowed to vary without explicit theoretical or experimental evidence.

Next, the fabrication process and structure of polysilicon and the practical aspects of its application will be reviewed. The polysilicon of this study is LPCVD grown, where LPCVD is an acronym for low pressure chemical vapor deposition. Thus the fabrication process involves placing an oxidized wafer in an evacuated furnace and heating the wafer, in this case to about 650 °C. Then, silane gas (SiH_4) is passed through the reactor, and the interaction of the silane with the hot wafer causes a reaction which deposits silicon in polycrystalline form on the surface of the wafer. This process can result in either amorphous or fine grained (100-500 A) polysilicon, depending on the temperature, pressure, etc. The polysilicon can be doped in situ by the mixing of dopant carrier gases with the silane, but this process was not used in this study, because it was desired to have the dopant control of the implant process. By chemically depositing this material, the process is very integratable with other integrated circuit (IC) processes, and this is a main advantage of the chemical vapor deposition (CVD). The process is carried out at low pressure so that the uniformity is improved and the deposition rate is reduced, and the process is better controlled. This material is gaining much acceptance in the IC industry for a variety of applications.

The first application of this material to find commercial use was for the gate material of metal-oxide-semiconductor (MOS) field effect transistors. The use of the poly-gate brought about the first self-aligned MOS processes, since the polysilicon on the gate can act as a mask for the source and drain implants, and withstand the implant activation temperatures. This step also dopes the polysilicon, which must be highly doped to reduce its series resistance and achieve the proper threshold voltage. As we will see, the minimum sheet resistance for 0.5um films is about 20 ohms per square, and this is becoming a limitation as device geometries are reduced. Heavily doped polysilicon can also used for short interconnect lines, has the advantage of being oxidizable, and also is available free when poly-gate is being produced. Again, the limitation is that the sheet resistance is much higher than metal lines, so the polysilicon interconnects are used for short lines only, such as interconnect within a memory unit cell. Another application of LPCVD polysilicon currently in production is the use of lightly doped polysilicon for load resistors in n-channel MOS (NMOS). In this case, it is desired to have a resistor with very high value (1 megaohm to 1 gigaohm) that does not require any wafer area. As we shall see, lightly doped polysilicon has very high resistance, but the resistance varys considerably from device to device, and the temperature coefficient is very large. For load resistor applications, these limitations are not disastrous. A new application of this material is for contacting bipolar transistors with shallow emitters. In this case, the heavy doped polysilicon is used because it creates a contact with low surface recombination velocity, allowing the shallow emitter to reduce its recombination losses. Another application is the use of polysilicon for fuses in programmable read-only memories (PROM) processes. The polysilicon is actually the programming element, which is either left in place or blown out to create the programming of ones and zeros at each memory location. This technique works because the polysilicon resistor can be made an open circuit by sending a very large current through its length. This technique is very much automatable, allowing for rapid programming of standard production parts. As can be seen, polysilicon is emerging as a very important addition to IC fabrication processes.

The one similarity in all the above applications is that the dopant density does not require precise control. For the application intended by this study, precise control is required. The IC resistor application needs a polysilicon resistor with about 1000 ohms per square and zero temperature coefficient. This is quite a difficult assignment for several reasons; the resistance of the polysilicon depends on the temperature cycle, and any IC process will include many high temperature steps set by other requirements of the process. Thus the properties are determined to some extent by the other process conditions, which probably cannot be modified to improve the polysilicon characteristics. As an example, modern MOS processes are kept to temperatures of 900 ^{o}C or less, while it will be seen that the polysilicon characteristics desired require

1100 ^{o}C temperature anneals. Also, it is desired to dope the polysilicon at the same time the source and drains are implanted, putting another constraint on the polysilicon process. In general, there are too many practical constraints to obtain the characteristics desired, which is why further study is needed. The polysilicon IC resistor will be the practical application for the work described in this study.

As discussed, this study investigates the electronic properties of polysilicon as a function of the process conditions. Special attention will be placed on the temperature function of resistivity, since this is of primary practical importance. The study was directed at determining the conduction-limiting characteristics and attempts to achieve better understanding of those characteristics. The major problem with polysilicon is nonuniformity. Being polycrystalline, it is characteristically nonuniform, yet most current models use only average parameters, as though the material were uniformly average. This basic approximation limits such characterizations for a simple reason: any functions involving distributed variables must be analyzed within the averaging process, otherwise, mathematically erroneous results will develop. As an example of a distributed variable consider the grain size L in polysilicon. Clearly, any realistic description would involve grains of various sizes [11,12,13], with relative percentages, and some average <L>. Now consider the total grain boundary area per unit volume as a function of grain size. The boundary area varies with grain size proportionately to 1/L, within a constant determined by grain shape. The total grain boundary area is thus proportional to $<1/L>$ where the average is taken over all the grains per unit volume. The result of the grain size's being a distributed variable is that $1/<L> = <1/L>$. The real value of $<1/L>$ will depend on the distribution function of the variable L. In this case, the result is that the smaller grains contribute more area than the larger grains, yet this information is lost when $<L>$ is used. The use of distribution functions can improve the accuracy of polysilicon modeling; however, it also increases the computational complexity. This study will incorporate distribution functions for the grain size and the grain boundary barrier heights into the formulation of a model for the resistivity versus temperature for this material.

The other problem area in the modeling of polysilicon involves the selection of parameters for inclusion in the model. The tendency in the literature is to use known results from single crystal silicon. An example of this is the routine interchanging of the dopant density with the majority carrier density, which is a good approximation for single crystal silicon but is not valid for polysilicon. In polysilicon, a substantial percentage of majority carriers is known to be permanently trapped at grain boundary defect states. Also, a substantial percentage of dopant may be trapped and inactive at the grain boundary. Thus, care must be taken in model development to accurately involve either the carrier density or the dopant density and to carefully assign its value. This project will show how to properly incorporate these variables, and use only appropriate values determined by experiment. A side effect of the mechanism of dopant segregation is that a profile must exist between the grain boundary dopant density and the bulk, constant dopant density. This study includes the effects of such a profile on the calculation of the trapped charge density. Overall, it is seen that care in parameter choice is very important, and these improvements will enhance confidence in this model.

These theoretical modifications are incorporated into the model for evaluating the resistivity versus temperature in polysilicon resistors. The resistivity as a function of temperature is especially interesting since it involves analysis of the transport properties of the polysilicon, and is a practical problem for the IC industry. The resistivity was found to vary approximately exponentially with temperature, with resistivity decreasing as temperature increases. This allows the possibility of thermal runaway, and is a serious problem. Also, the parameters of resistance and its temperature variation are extremely sensitive to process variables, notably the dopant density and the thermal history. This investigation will apply the developed model to characterize the measured resistance versus temperature on a selection of polysilicon samples, where the doping density and annealing temperature are varied over the entire useful range. The goal is to obtain a correlation between the distribution function parameters, which are determined experimentally, and the known process variables. Analysis of experiment will result in estimates of resistance, barrier heights, trap density, carrier density, grain boundary area and dopant segregation for each element of the process matrix. The LPCVD polysilicon thin film resistors used in this study were fabricated at Harris Semiconductor.

CHAPTER II

REVIEW OF CURRENT THEORY

Polysilicon has been known as an important electronic material for many years [1,2,3,14]. Experimental results [11,15,16,17,18] show a significant difference in the electrical and transport properties of polysilicon compared to single crystal silicon material. Several models have been presented as potential theories to explain these properties [1,5,7,19]. Clearly, the presence of grain boundaries is the dominant factor influencing conduction in polycrystalline material. The electronic effects of grain boundaries are still being debated, with primarily two main theories central to the discussion. This work will address these theories as part of the study. Another aspect of any work on polysilicon involves the natural nonuniformity of this material; as a result, variables are so sensitive to structure and process that most models have limited application range. Also, some physical "constants" of single crystal silicon may or may not be usable in polysilicon formulations. In general, any model must involve limiting assumptions which should be carefully evaluated for the work to be useful.

The experimental work to be explained by these theories include the properties of a first order characterization of conduction mechanisms: the dependence of resistivity and mobility versus temperature and doping density. These basic parameters have unique behavior characteristic of polycrystalline material: resistivity is found to be an extremely steep function of doping and temperature, especially in the medium doping range, and mobility has a drastic minimum at a doping density in this range [1,4,6,18]. The exact values where these effects occur depend very sensitively on the process received by the polysilicon and the details of microstructure and thermal history, etc. It might also be conjectured that the results depend on the laboratory where the depositions and measurements were performed and the details of their procedures. Since the material is inherently nonuniform, scatter between samples may be considerable and is unavoidable. Such a wide range of resistance values is encountered that experimental equipment limits may be reached. It is seen that the simple conduction experiment is not simple at all, and the results are very interesting.

Several physical models have been developed in attempts to explain the properties of grain boundaries [1,5,7]. The main concepts behind these models are grain boundary trapping and grain boundary dopant segregation. The trapping model assumes that the boundary has many "dangling bonds" or other defect structures that trap majority carriers permanently in a sheet of charge at the grain boundary, creating a potential barrier which inhibits further conduction [6]. The segregation model assumes the strain fields associated with the boundary trap and deactivate dopant atoms as they diffuse along and through the grain boundaries [7]. Although both models result the presence of fewer free carriers in the material, the physical mechanisms are different and there is enough difference for experiments to indicate either mechanism. Indeed, both models have experimental support which suggests strong influence. The present work will address both these models in the analysis of the experimental results. Many researchers also include tunneling into the theoretical description of grain boundary behavior [7,9,10,19]. These models involve more complex characterization of the boundary barrier, with a tunnelling or scattering barrier that is independent of the potential barrier created by the trapped charge. This boundary is usually identified as a layer of amorphous silicon or silicon oxide which has a much higher energy gap and is very thin. It is noted that the properties of this tunnelling barrier are hypothesized and cannot be verified. Another problem with the tunnelling theories is that most formulations require these physical parameters to be temperature dependent to reach agreement with the experimental results of resistivity versus temperature. Also, there is no definitive evidence of the material or structure of this boundary layer, and the tunnelling formulation requires several strict assumptions to be obeyed, such as the boundary layer's being thinner than 50 A. Still another mechanism that has been proposed is the hopping current model, where electrons cross the boundary by hopping from one defect state to another. This mechanism occurs with a different activation energy, and thus these formulations extract two regimes with different energies for the thermionic emission and the hopping current from the temperature characteristics. Although these complex formulations may be appropriate in some cases, such as a single boundary with a large forward bias, this study will show that that the thermionic emission process is adequate to characterize the resistivity versus temperature properties of the material being studied. The mechanisms of trapping and segregation will be developed into a new model for characterization of conduction mechanisms in polysilicon.

The Grain Boundary Trapping Model, much modified, has gained much acceptance in describing transport properties in polysilicon. This is due to the significant experimental support: the exponential dependence of resistance with temperature. The trapping model assumes that the majority carrier charge is trapped in defect states at the grain boundary, resulting in a potential barrier to carrier conduction across the boundary. The height of the barrier is determined by the density of charge at the grain boundary, and the density of ionized dopants in the depletion layer. Conduction is accomplished by thermionic emission over this barrier, in the sense of a Schottky barrier in forward bias. The Schottky barrier saturation current is known to involve a term of the exponential of the barrier height divided by the thermal voltage, which describes the thermal activation of this process. Thus, this thermionic emission mechanism gives the resistivity variation its characteristic exponential dependence on temperature. It is noted that the segregation model cannot explain the exponential dependence of resistivity on temperature. The trapping model can also explain the rapid decrease in resistivity with increasing dopant density if the total number of grain boundary traps is of the order of the dopant density at which the large decrease occurs. At lower doping, almost all the carriers are trapped, leaving no free carriers for conduction, and a very high resisitivity. As doping is increased beyond the point of filling all traps, the resistance declines very rapidly, due to the presence of free conduction electrons coupled with the Debye screening of the potential barrier. Since both the areal density of traps at the boundary and the total area of boundary can change with process, doping, and so on, this model can also qualitatively explain these process trends. Although this model has good potential for explaining experiment, the series of approximations required to analytically use it have restricted the quantitative accuracy of its application.

The theory of grain boundary dopant segregation also has solid experimental support in the dependence of resistance on anneal temperature and dopant specie [7,20,21]. That phosphorus atoms thermodynamically prefer the grain boundary is well established [22]. Studies have explicitly shown segregated phosphorus atoms at the grain boundary by electron microscope techniques [23,24]. However, the explicit percentage of dopants to segregate is still open for discussion, and will be addressed by this study. Also, the fact that this formulation has ignored trapping is selflimiting. The normal routine has been for segregation studies to assume dominance over trapping and vice versa. This study will attempt to include both segregation and trapping into the mathematic calculations. The theory of dopant segregation has another primary assumption, namely that the segregated dopant atoms are neutral and thus do not provide an electron for conduction. This assumption will be investigated by accounting for all electrons which exhibit themselves in the electrical properties, through the calculation of the majority carrier census. If the dopant atoms do segregate, then the solution of the diffusion equation will require the presence of a profile in dopant density from the boundary value to the bulk value. Such a profile will have a direct influence on the relationship between the grain boundary barrier height and the boundary trapped charge. This effect is included in our model for the first time, and explicitly shows the interaction of the segregation and trapping models. Also, the theoretical formulation of the segregation model involves several constants, particularly the total number of grain boundary states, which could be re-evaluated. Since this theory must share dominance with trapping, it is expected that its importance will be less than was predicted by Mandurah, et al [7,22]. The theory of dopant segregation will be considered in this study, and an analysis of the indications from the model calculations will be presented.

The use of the carrier trapping model must involve careful analysis and parameter use. In particular, it is desired to be practical, so the use of directly measurable quantities is of great importance. The first measurement to consider is the dependence of resistivity on temperature. The thermionic emission mechanism predicts Arrhenius behavior (i.e. exp E_a/kT), which is approximately but not exactly observed. Thus, the model must be refined to account for the deviation from pure exponential. Let us note that the deviation from the classical model is slight, and should not be taken as casting doubt that the thermionic emission mechanism is dominant. The first modification to consider is the temperature dependence of the pre-exponential factor, which for a Schottky barrier has a T^2 dependence. This factor has been assigned several potential T^x dependencies by different authors, with mixed results [8,13,17,18]. This project analyzes this pre-exponential factor in a later section and arrives at a T^1 dependence, which arises from the voltage dependence of the boundary. Another way to explain the non-Arrhenius behavior is to include the tunneling mechanism in addition to thermionic emission [7,10,25,26]. Several formulations of tunnelling effects have been proposed, each with its own temperature dependence, and these models involve the summation of thermionic emission and one or more tunnelling terms. The tunnelling models require the boundary to have another barrier, which is independent of the potential barrier created by the trapped charge. This barrier is usually identified as a layer of amorphous silicon or silicon dioxide, with a very large energy gap and very thin thickness. Unfortunately, tunnelling formulations are very complex, with abstract assumptions and too many parameters which do not correspond to measurable entities and must be a function of temperature. No work has identified undeniable reasons why the tunnelling formulation must be used for the case at hand. Recently, Thomson and Card [27,28] presented another explanation of non-Arrhenius behavior: that a distribution of barrier heights exists rather than a single, uniform barrier height. They showed that this distribution will result in an apparent barrier that seems to vary with temperature, thus creating the curvature observed in real data. Since polysilicon is a very nonuniform material, it is expected that such a distribution must exist, and there is experimental evidence that this is the case. This theory is conceptually much more pleasing than the tunnelling theory, since now the deviation from ideal characteristics is attributed to the nonuniformity of the material. The model of Thomson and Card is modified and developed into a model for the resistivity of LPCVD polysilicon in the next section. This model for the resistivity, including the distribution function formulation, is the primary endeavor of this study. The modifications to the Card model which are used to develop our formulation will be discussed in detail.

Once the potential barrier characteristics are extracted from the resistance function of temperature, the relation between potential barrier and trap density can be considered. This equation will be used in the calculation of the majority carrier census. A conventional Gauss' law calculation shows this relation to be

$$V_d = q\ N_t^2/8\ e\ N_d \tag{2.1}$$

where N_t is the areal density of trapped charge, and N_d is the total dopant ion concentration, which is assumed constant [16]. This last assumption is questionable in light of the undisputed dopant segregation, and a more advanced formulation has been developed by this study. This analysis concerns the effects of a nonuniform profile in the dopant ion concentration as the boundary is approached. It is seen that an increasing profile toward the boundary will result in a lower barrier for fixed charge, in the sense of Debye screening. In our work, the barrier height is the known parameter since it is determined from experiment, and the profile effects require additional charge to be trapped at the grain boundary. The exact magnitude of the effect depends on the profile. The profile is determined by a solution of the diffusion equation, as reported by Gilmer and Farrell [29]. This work shows the form such a solution will follow, though exact results are not possible due to approximations required in the diffusion constants. From this work it is seen that the transition profile is quite steep, and is closely approximated by a linear function. Chapter 5 will show the general formulation for the inclusion of a dopant profile towards the grain boundary, and the majority carrier census will include the calculation of this effect for the assumption of a simple linear grade. Also, the relative dielectric constant may be a function of dopant density or local defect density, but no reliable information is available [30]. The relation of grain boundary charge to voltage will be used to evaluate the areal density of trapped charge, being careful not to assume this is the total trap density.

The next relation to be considered is that of areal charge density to total volume charge density. Clearly, the proportionality is just the total grain boundary area per unit volume. This factor depends on the shape, size and distribution of the grains. Current models assume cubic grains, all of avarage size, to get total grain boundary area [7,9], which is not adequate. The shape of the grains determines the area/volume ratio, but real grains do not occur in simple geometric shapes. It is difficult to evaluate the validity of using a shape close to actual structure, such as cylinders. For a given shape, the area/volume ratio is evaluated as a function of grain size. This becomes the function which must be integrated over the entire grain size distribution to get the appropriate average. Since the area/volume ratio is proportional to 1/L, the small grains contribute more boundary per volume than the larger grains. This nonlinearity invalidates any treatment based on an average grain size. The corrected form of the parameter (grain boundary area) will be included into the calculation of total trapped charge and into the calculation of grain boundary segregation.

A final area of theoretical concern is the interpretation of Hall effect measurements. In order to use the Hall effect, assumptions must be made concerning material properties and constants. For the small grain sizes in this project, the Hall results give a good estimate of the carrier concentration inside the grain [31]. Thus, the Hall effect measurements will be used for determining carrier density for concentrations up to 10^{20} cm^{-3}. Note that the heavy doping effects must be considered, in particular the variation of the Hall constant r_H with doping density. All previous workers have used $r_H=1.0$ which is not valid for high doping. This work will use the heavy doping value, $r_H= 0.9$, for densities $>10^{19}$ cm^{-3} [32]. This factor will introduce a numerical change, especially when analyzing the relative effects of trapping and segregation.

Another area of concern in the Hall Effect measurements is interpretation of the mobility which is obtained. Even in single crystal material, there is some discussion about what the Hall mobility actually corresponds with, and its relation to the drift and conductivity mobilities. In polysilicon, the interpretation requires even more abstraction, since there are several mechanisms which influence the value of the mobility. For example, whether this mobility is representative of the bulk of the grains or of the grain boundary depletion region is of primary concern, since these values will enter into the formulations in different ways. In the classical Ohm's law formulation, the conductivity should equal the mobility times the carrier density times the electronic charge, and this is the basis of the extraction of the mobility from the Hall Effect measurements. One of the results of this work is that this form is maintained, but the mobility in this expression cannot be related to any kind of physical charge motion since it also involves the thermal activation of transport over the grain boundary barrier. This is explicitly apparent because the carrier density is constant over temperature in the experiment results, meaning that the thermal activation which is well known in the resistivity must also be the temperature function of the mobility. However, in the Schottky theory upon which the thermal activation is based, the mobility which is used is the bulk crystal value and the thermal activation is a separate function. The net result of this analysis is that the mobility obtained from the Hall measurement is an effective mobility only, in the sense of Ohm's law, and does not directly correspond with the physical conduction mechanism.

In this section, the basic theories of trapping and segregation and their assumptions have been discussed. It is seen that these models can be used to explain observed experimental results. It is also seen that these models involve many assumptions, some of which are to be modified to achieve a more realistic characterization of conduction mechanisms in polycrystalline silicon.

CHAPTER III

MODELING OF NONUNIFORMITY

Before the resistivity formulation can be described, the averaging process for distributed variables will be derived. A distributed variable is one which takes one of any number of different values at different times. In the case of polysilicon, the distributed variables are those whose parameters change at different locations in the material. With such variables, care must be taken to average properly or errors will result. To perform the average, you must first analyze the effect of the variable in the formulation, since an expression must be written to describe the action of the variable in the desired equation. Then, the expression is multiplied by the distribution function and integrated over the range of values of the distributed variable.

As an example, consider the grain size in the polysilicon, which has already been described as a distributed variable. However, it is not the grain diameter or radius which is desired, but rather the grain boundary area, which is related to the grain diameter and is inversely proportional. Thus the expression to be integrated is not L, the grain diameter, but 1/L. The proper average will be <1/L>, which is calculated by

$$\langle 1/L \rangle = \int_{0}^{\infty} a(L)(1/L)\,dL \tag{3.1}$$

where a(L) is the distribution function of the grain sizes. The important result is that the grain boundary area is proportional to <1/L> and not to 1/<L>, which would be different. This result for the grain boundary area is related to the surface-to-volume ratio by a proportionality constant, which depends on the shape of the grain. This study assumes a unity proportionality, which gives a conservative estimate of the surface-to-volume ratio. The values for this constant will be determined experimentally by transmission electron microscopy (TEM).

The expression inside the integral is called the weighting function, and thus the average over a distributed variable is calculated by multiplying the distribution function by the weighting function and integrating over the entire range of the distribution function. It is noted that the distribution function should be normalized. This mathematical procedure is the key to the model developed by this study.

The general formulation is now explicitly related to the variables of interest to this study. The first parameter is the grain boundary area which has just been discussed. In this case, the expression describing the relationship between the dependent variable (grain diameter) and the desired result was an inverse function. The next application of this process is to properly average the effects of various grain boundary heights in the formulation of the temperature dependence of resistivity. Results fromthe literature [16,33] indicate that the barriers will be different locally, thus we need to apply the techniques for distributed variables. The expression in which the barrier height appears is the description of the process of thermionic emission over the barrier in question. The weighting function for the thermionic emission mechanism is the classical exponential for any thermally activated process. This expression is the origin of the severe temperature dependence of the resistivity. Here the averaging integration process is written:

$$\exp(-V_{do}/V_t) = \int_0^\infty a(V_d)\exp(-V_d/V_t)dV_d \qquad (3.2)$$

and it is seen that the previous relation including only the average barrier height will be replaced by the properly integrated average. This will be discussed in detail in the next section, and the result will be that the distribution function integration gives an additional term, involving the standard deviation, which makes the equation deviate from the strict exponential function. It is seen that the exponential weighting function makes the average very sensitive to the distribution function properties. In this study, a Gaussian distribution function will be assumed for the barrier heights, for tractability of integration, but this is shown in Chapter IV to be the result of the first additional term of a Taylor expansion of the general function form of the temperature dependence of the barrier height. The barrier height formulation and the grain size/boundary area term are the primary usages of the distribution function averaging included in this model. These are not the only possible applications of this process, however, since polysilicon has more variables that can be described as distributed in nature. Also, further implications of the distributed variables already mentioned do exist. For example, the barrier height has an important relationship to the amount of trapped charge at the grain boundary, and this calculation is performed in the majority carrier census. In the classical case, the formula is written:

$$V_d = qN_t^2 / 8 e N_d \tag{3.3}$$

but the barrier height is now described through the distribution function, and this expression must be modified to properly account for the distributed properties. To analyze the weighting function, the relation is rewritten to show the desired result as a functional of the distributed variable. Here, the trap density N_t is written as a function of the barrier height:

$$N_t = (8eN_dV_d/q)^{1/2} \tag{3.4}$$

and this function must be integrated over the distribution function of barrier heights.

$$\langle N_t \rangle = \int_0^\infty (8eN_dV_d/q)^{1/2} \, a(V_d)dV_d \tag{3.5}$$

which gives the true average trapped charge density at the grain boundaries. Notice that this case involves a weighting function that exhibits a square root dependence on the distributed variable, while the previous case was exponential. Thus, the effects of the integration are much less for the trap density; indeed, our calculations show that the classical approximation will result in less than 1% error for this case. This formula, the relation between trapped charge density and barrier height, is discussed in much detail in later sections, including the effects of a dopant profile.

In summary, the mathematic procedure for proper averaging in the presence of a distributed variable has been described. It is seen that for the case of polysilicon, two important applications of this process are apparent, that of the barrier heights and that of grain sizes. These functions are sensitive to the average process because their weightings are steep functions of the distributed variable; exponential and inversely proportional, respectively. This procedure is very important for the model developed in this study.

CHAPTER IV

MODELING OF POLYCRYSTALLINE SILICON FILMS

In this section, the resistivity model will be developed in explicit mathematical detail. The derivation should begin from first principles, which for a resistivity derivation should involve the expression of the current-voltage relationship of the primary conduction mechanism. For a uniform resistivity material this would be an Ohm's law formulation. For polysilicon, it has already been discussed that the limiting conduction mechanism occurs at the grain boundary by the trapping of charge and the creation of potential barriers. In the model of this study, it will also be assumed that conduction is dominated by the process of thermionic emission over the grain boundary barriers. Thus, an adequate starting position is the equation for the J-V dependence of a single boundary reported by Thomsonand Card [27], where the use of distribution functions for barrier heights was first introduced. This work was for a special device structure, and many modifications are necessary for application to the case of LPCVD polysilicon. These modifications and the new assumptions and formulations are presented in this chapter.

In a recent paper, Thomson and Card [27] reported a study of the conduction process across the grain boundary barrier in a silicon bicrystal. Their observations indicated that conduction across large grain boundaries was spatially nonuniform in some cases. The model they developed was based on the thermionic emission theory and included the effect of the grain boundary barrier height's variability across the area of the grain boundary. They described the transport across the barrier of their study by their equation (2):

$$J = qN_c uE_m/2 \exp(-\varnothing_b/V_t)\exp(V_1/V_t)(1-\exp(-V/V_t)) \qquad (4.1)$$

where N_c is the density of states in the conduction band, u is the mobility in the depletion region, E_m is the maximum electric field in the space charge region, $\varnothing_b$ is the activation energy, V_t is the thermal voltage in electron volts, and V_1 and V are the applied forward and total biases on the barrier. This equation has been derived from a reexamination of the basic thermionic emission process. The analysis that constructs the Richardson constant has been revisited and the mobility and electric field terms are the replacement for the Richardson constant. The exponential terms derive from the thermionic emission across the barrier and its applied voltage dependence. As yet, this equation does not include the distribution function, which will be introduced by a substitution for the activation energy $\varnothing_b$ soon. The equation, as presented, is not useful for the case of LPCVD polysilicon in this form, but does contain a description of each process required for the model that will be developed. The modifications will now begin:

4.1: Barrier Height

The $\exp(\O_b/V_t)$ expression in the above equation is the classical formulation of the thermal activation of the thermionic emission process, with $\O_b$ being the barrier over which the carriers are thermally activated. As seen from the band diagram, Figure 4.1, the $\O_b$ term is actually the sum of two terms, the first being the actual band bending, or barrier height, V_d, and the other being the bulk fermi level, defined here as $V_n = E_c - E_f/q$. Each of these terms involves more discussion, so they will be discussed separately.

The V_d term is the grain boundary barrier height and in the classical form represents the average barrier in the material. The improvement for this term is to write a substitution based on the distribution theory to reformulate the thermionic emission in the distribution function form. The weighting function will be the exponential expression which relates the thermal activation of the thermionic emission mechanism. Following Thomson and Card (eq. 5):

$$\exp(-V_{do}/V_t) = \int_0^\infty a(V_d)\exp(-V_d/V_t)dV_d \qquad (4.2)$$

where this equation indicates that the term involving the average barrier height is to be replaced by an averaging integral over the distribution function of barrier heights and the weighting function which shows the action of the barrier height in the overall problem. This is the proper way to perform the average over the distribution function as described in the preceding chapter. The distribution function used in this case will be a standard Gaussian:

$$a(V_d) = (2\pi\sigma)^{-1}\exp((V_d-\langle V_d\rangle)^2/2\sigma^2) \qquad (4.3)$$

where $\langle V_d\rangle$ is the average barrier height and σ is the standard deviation of the barrier height distribution function. It is noted that the use of the Gaussian distribution function is equationally identical to performing a Taylor series over the barrier height function of inverse temperature and taking the first two terms. This interpretation leads to some questions about the definition of the "average" value of barrier height, since the Taylor series expansion would have different physical meaning. The Taylor expansion formulation will be presented and discussed below. The integration over the Gaussian times the thermionic term can be performed, through the use of the standard form for the integration of a quadratic exponential. The result of this integration is the following explicit substitution:

$$\exp(-V_{do}/V_t) = \exp(-\langle V_d\rangle/V_t + \sigma^2/2V_t^2) \qquad (4.4)$$

as long as the inequality $\sigma/V_t < \langle V_d\rangle/\sigma$ holds. This inequality allows the simplification of an erfc term with the difference of these terms as the argument. The negative argument case simplifies nicely to a value of 1/2. This inequality has been found to always hold by the works of Thomson and Card and this study. If the inequality does not hold, there is certainly no easy way to extract the parameters desired for this procedure. It is noted that cases probably do exist where the inequality does not hold, but they have not been encountered by this study. It is seen that the above result shows that the variation in grain boundary barriers causes an additional term which involves the second power of the inverse thermal voltage to be added, and the form of the temperature function will no longer be a strict linear exponential function. This is an important result, since now the variation from ideal terminal characteristics is directly attributed to the nonuniformity in the material. As previously discussed, this is an alternative concept to the prevailing concensus that the deviation from ideal thermionic emission is caused by the tunnelling mechanism.

Next, an alternative derivation will be presented which arrives at the same expression for the barrier height function from different assumptions. This will be a Taylor series expansion, which proceeds in much the same way as the data analysis procedure. It will be shown that this alternative derivation results in a different assignment for the term presently called the average barrier height.

To perform the Taylor series expansion, we begin with an arbitrary expression for a thermally activated resistivity. For example:

$$R = R_o \exp (E_a/qV_t) \qquad (4.5)$$

In the classical thermionic emission theory, we would write (see band diagram, Figure 4.1):

$$E_a/q = V_d + V_n \qquad (4.6)$$

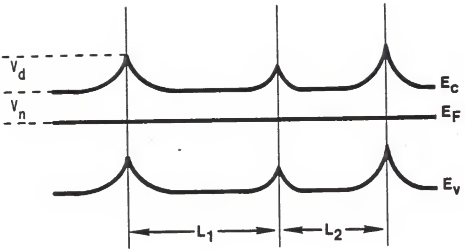


Figure 4.1: Band diagram for polysilicon material at an arbitrary location. Notice that both the grain size and the barrier height are variable.

and then take the derivative to get

$$\frac{d \ln R/R_o}{d\,(1/V_t)} = E_a = \frac{d\,(\,V_d/V_t + V_n/V_t)}{d(1/V_t)} \qquad (4.7)$$

taking the first term of this expression

$$\frac{d}{d\,V_t^{-1}}\,\frac{(V_d)}{(V_t)} = V_{do} + \frac{1}{V_t}\,\frac{dV_d}{d\,V_t^{-1}} + \ldots \qquad (4.8)$$

which is a Taylor expansion of the variable V_d into $1/V_t$. In this expansion, the first derivative term will correspond to the standard deviation expression in the distribution function model through the substitution

$$\frac{d\,V_d}{d(1/V_t)} = -\sigma^2 \qquad (4.9)$$

and higher order terms in the Taylor expansion are neglected. The result is that the Gaussian distribution function model and the Taylor series expansion are similar explanations for the same observation; it is seen that the Gaussian distribution function arises from a logarithmic Taylor expansion. The Taylor expansion could be carried to additional terms, but a much more complex distribution function would be required, and the physical understanding of each term would be difficult. In this expansion into Taylor series, we see explicitly that the term V_{do} might be called the "average" in the Gaussian distribution description, but corresponds to the value of the function at the argument of zero in the Taylor expansion. Thus, this value of barrier height would be exhibited in the terminal characteristics only when the inverse temperature is zero, or the temperature is infinite. What is not clear is whether the charge density indicated by the "average" is not also the correct value only when the temperature is infinite. This would be the case (infinite only) in the average barrier (classical) model, but in our procedure, we integrate over the distribution of barrier heights to get the charge density, which should be correct. The only remaining question is then that part of the distribution function which has barriers larger than the average, which would never be observed in the terminal characteristics. The other aspect of this discussion is trying to correspond to the current practice in the literature, where only the average statistics are used. The choice between these two explanations is philosophical and is thus difficult to make. The study will continue by reporting both the Gaussian parameters of average and standard deviation, along with the room temperature barrier height assuming the Taylor expansion definitions. Troom temperature statistic will be used to compare with the previous results in the literature, since the other values have different meanings. Again it is seen that there are always further implications of every assumption made in the modeling of polysilicon properties.

4.2: Carrier Density

In expression (4.2) the Fermi level, V_n, was separated out of the activation energy by explicitly subtracting the barrier height.

The V_n term is now grouped with the N_c term to form an expression for the carrier density N, in the bulk of the grain:

$$N = N_c \exp\left(- V_n/V_t\right) \tag{4.10}$$

This is the classical Maxwell-Boltzmann formulation of the carrier density in terms of the Fermi energy and the density of states in the conduction band. This relation is also equated to the dopant density in single crystal silicon, through the assumption of complete ionization, but this approximation is not valid in polysilicon. As mentioned, for this case, there is a difference between the dopant density and the carrier density, and the Fermi level must be explicitly related to the carrier density. The value of the carrier density N, in the grain bulk, is determined experimentally from the Hall Effect measurement. The results of this investigation show that the carrier density in the bulk of the grain is constant with temperature (see section 7.5), so that the resistivity function of temperature is due to other factors. Since the parameter extraction process involves temperature derivatives, the derivative of V_n is also taken into account, and results in a correction term of $3V_t/2$ in the barrier height calculation. This is derived next.

For this derivation, we return to (4.7) for the remaining term in the Taylor expansion of the activation energy, the Fermi level term:

$$\frac{d}{d\,1/V_t}\left(\frac{V_n}{V_t}\right) = V_n + \frac{1}{V_t}\,\frac{dV_n}{d\,1/V_t} \tag{4.11}$$

which is just a chain rule expansion of the derivative. Next perform a change of variable from d $1/V_t$ to dT to get

$$V_t = kT/q \quad \text{so} \quad d\,1/V_t = -q/kT^2 \;\; dT \qquad (4.12)$$

and thus

$$\frac{1}{V_t}\frac{d\,V_n}{d\,1/V_t} \;=\; -T\,\frac{d\,V_n}{d\,T} \qquad (4.13)$$

using the simple Maxwell-Boltzmann expression for the Fermi level:

$$V_n = kT/q \ln\,(N_c/N) \qquad (4.14)$$

and the classical $T^{3/2}$ dependence of N_c [34], along with our experimental result that the carrier density is constant, results in

$$-T\,\frac{dV_n}{dT} \;=\; -V_n - 3V_t/2 \qquad (4.15)$$

and collecting all these terms (4.8,4.9) gives

$$\frac{d \ln\,(rho/A\;V_t)}{d\,1/V_t} \;=\; E_a = V_{do} - \sigma^2/V_t - 3V_t/2\;. \qquad (4.16)$$

Thus we see that three terms are involved in the activation energy, the average barrier, the standard deviation of the barriers, and a calculated term which results from the dependence of the Fermi level on temperature, which is $3V_t/2$. Thus, an activation energy of zero, or a flat temperature function of resistance, will still have a barrier of $3V_t/2$, which is needed to offset the Fermi level term. This is the explicit model for the activation energy which was used to perform the calculations of this study.

4.3: Linearization

This section examines the voltage dependence of the current in the expression (4.1) with the goal of obtaining a trustworthy equation for this function. In the first expression from Thomson and Card above, the voltage dependence is expressed through the double exponential term in V_1 and V_2, the biases across the two sides of the grain boundary. In the study of small grain polysilicon, it is not possible to determine the individual boundary voltages, so an assumption must be made concerning these voltages in order to continue. In this case, the conventional form will be used and the voltage dropped across each side of the barrier will be assumed to be equal. This approximation, though standard, is not intuitively obvious. As long as the applied bias at each barrier is small, the approximation is valid. The definition of a small bias on the barrier is that the applied voltage at any barrier be less than the thermal voltage. This condition is satisfied by the fact that each sample contains thousands of barriers. It is noted that the model being presented is thus designed for the "zero-bias" conditions, so that the problems of strong forward bias are avoided. The large signal behavior of grain boundaries has been studied by other workers [35,36,37] and is found to be quite complicated. This assumption makes the argument of each bias exponential the same, and leads to the standard sinh form for the current-voltage relationship across any boundary [5,22,38]. It is also necessary to make the further assumption that the terminal voltage is the series addition of many boundary voltage drops which are all about equal, namely $V = N_g V_g$, where V_g is the average drop across any grain and N_g is the number of grains between contacts. This results in an I-V relationship as follows:

$$I = I_s \sinh (V/2N_gV_t) \ . \tag{4.17}$$

This form is the foundation of much work by many authors in attempting to characterize the material through the "electrical effective number of grains" N_g [5,38]. The process they use is to measure the characteristics at high voltages so that the sinh form is observed, and then extract the N_g term from the slope of the I-V characteristics on a semilog plot. It is necessary to measure the currrent-voltage relationship to biases of one hundred volts to observe the sinh form. This has been attempted by this author without success. As mentioned, the assumption of equal barrier drops is questionable at large forward bias, but many reports have used this model with success [5]. The primary reason the results of this work do not support this model is that the number of grains extracted from this measurement does not scale properly with the length of the resistor. Simply, a resistor twice as long should have twice the number of grains, but this was not the case for the resistors available. In addition, the sinh form is not observed by the results of this study. These data will be presented in the section 7.5. In this study we will make the further assumption that the voltage drop across any boundary is smaller than the thermal voltage, so that the sinh term can be expressed in its low voltage approximation, namely as a linear function:

$$\sinh (V/2N_gV_t) = V/2N_gV_t \ . \tag{4.18}$$

Thus, the resistivity will be determined only in the linear region of the I-V function. This limitation practically requires keeping the applied voltages in the range of 20 volts or less, and thus is not a very strict limitation because these devices contain so many grain boundaries. Thus, the equation is now

$$J = (qN/4\ N_g)\ \exp\ (-E_a/qV_t)\ V/V_t \tag{4.19}$$

where E_a contains all distribution function terms.

4.4: Resistivity

It is now possible to complete the development of the resistivity by converting from the J-V relationship to an expression for the resistivity. This is accomplished through the assumption that all the voltage is dropped across the grain boundaries rather than in the bulk of the grains. It is recognized that this assumption may be somewhat limiting, but will impose serious problems only at high doping levels when the boundaries are not very high. In these cases, the thermionic emission model loses validity for other reasons also, so this assumption of the drop across the boundaries is not much additional limitation. This relation is basically Ohm's law and is expressed

$$J\ (\rho)\ L = V \qquad \text{or } J = 1/(\rho)\ \ 1/L\ \ V \tag{4.20}$$

at each grain, so that, following the averaging process,

$$\rho = \langle 1/L\rangle V/J \tag{4.21}$$

This equation expresses the fact that that the current density J flows across the total area of grain boundaries present in the material. This total area of boundary can be converted into the surface-to-volume ratio by including the N_g term and releasing a constant to the prefactor. This allows the use of the experimentally determined constant, the surface to volume ratio, in expressing the grain size dependence in both the calculation of the majority carrier census, and in the resistivity model for the material. It is seen that the final expression is now

$$R_s = (N_g/uE_m)(4V_t/\ q\ N)\ S_v \exp\ (E_a/qV_t). \qquad (4.22)$$

The important aspects of the model can now be seen explicitly, that the exponential prefactor has a linear T dependence in the V_t term, that the resistivity is inversely proportional to the carrier density N in the Ohm's law tradition, that the resistivity is proportional to the total area of grain boundaries, and that it varies according to the exponential dependence resulting from the grain boundary distribution statistics.

The final modification to the resistivity model concerns the constants grouped in parentheses above. These constants are those which involve further assumptions concerning the material parameters which cannot be determined with certainty. The values of u and E_m could be approximated from single crystal silicon values, and the value of N_g could be extracted from the sinh function, but these techniques are not considered to be trustworthy by this author. Therefore, these constants are grouped together into a single constant R which is actually correspondent to the Richardson constant in the classical Schottky theory [27,34,39]. This constant will be determined from the experiment data of resistivity after all the other constants have been determined. The final expression for the resistivity model developed by this study is thus

$$R_s = (4\ V_t\ R/\ q\ N)\ S_v \exp\ (E_a/qV_t)\ . \tag{4.23}$$

Now all constants are either known physically or determined experimentally. This model inspires more confidence than previous models where many parameters are uncertain and may need to depend on temperature.

In summary, a model for the resistivity of polycrystalline silicon has been developed by reconsidering the many assumptions required to determine their applicability to the case under consideration and a new formulation for the resistivity in this material is presented. The important contributions of this model include the following.

This study introduces the use of the distribution function of barrier heights to model the temperature function of resistivity. This formulation explicitly relates the deviation from ideal thermionic emission to the nonuniformity which is known to exist in the polysilicon material.

This study shows the proper use of the carrier density rather than doping density in the formulation of the resistivity. Since the two variables are different in polysilicon, this modification is more accurate and returns the expression to the Ohm's law form.

This study introduces the use of the grain size distribution function in the formulation, which will correctly include the influence of the small grains. Now the resisitivity is proportional to the area of grain boundary area which must be crossed for conduction to occur.

The final factor that improves confidence in this model is the exclusive use of known or experimental constants which are independent of temperature. This modifications will remove much of the uncertainty associated with models that rely on uncertain constants.

These modifications are important for practical and conceptual reasons. Now there exists a model where the characteristics of the material can be characterized completely by experimentally determined parameters. This model can also improve the understanding of the important parameters which determine the electrical properties. Also, the formulation has been chosen to focus the attention on those properties which are important, namely the nonuniformity of the usual parameters of conduction. This model will be applied to the experiment results, and all the parameters will be calculated and discussed, in the remaining chapters.

CHAPTER V

MAJORITY CARRIER CENSUS

The next discussion will be of the procedure for calculation of the amounts of charge present at the various sites available, which will be referred to as the majority carrier census. This calculation is very important since the assumptions as to the various possible physical mechanisms must be based on the relative amounts of charge involved. For example, the theory of dopant segregation [7,22] assumes that this effect is dominant over carrier trapping while the carrier trapping model makes the opposite assumption [5,9]. The experimental evidence indicates that both processes occur [5,15,20,23], but their relative contributions are still under discussion, and this is one of the reasons for the majority carrier census. Another has been previously mentioned, namely that the carrier density and dopant density are not the same locally, and this difference has further implications which need to be investigated. The majority carrier census will be described, and the implications of our modeling on these parameters will be discussed.

The goal of this procedure will be to determine the location of the various charge subsets through examination of experiment data. The models used to calculate the charge subsets from experimental results are sensitive to the many assumptions that must be made to arrive at an analytic formulation for all the subset densities.

Part of the value of the majority carrier census is to explicitly express these assumptions and their implications in the calculation. Thus, this section will investigate each relationship with the goal of improving the realism of the calculation for the case of the polysilicon material under consideration. The first function to be considered is the grain boundary barrier height relationship to the amount of charge trapped at the boundary. This relationship is fundamental to the theory of grain boundary trapping. In its conventional form [5], it is written as

$$N_t = (8\ e\ V_d\ N_d\ /\ q)^{1/2} \qquad (5.1)$$

where the N_t is the total trapped charge at the grain boundary, V_d is the barrier height, N_d is the dopant density, and e is the dielectric constant of silicon. This is the equation used to extract one subset of the majority carrier charge, being that trapped at the grain boundary. Notice that this equation determines the charge density at the grain boundary from an experimental result, the barrier height. The other subset of the majority carrier charge is the free carriers, which is determined directly from Hall Effect measurements. The sum of these terms should be the total density of majority carriers in the material. This sum is set equal to the number of ionized dopants by the principal of charge neutrality. The difference between the number of ionized dopants and the implanted phosphorus density is an estimate of the number of phosphorus atoms that are inactive. The calculation of these "missing" or inactive donors has been used in this study to estimate the density of segregated phosphorus atoms. This relatively simple procedure nonetheless involves many serious approximations which greatly affect the numbers in the various subsets. It is a goal of this study to calculate each of these subsets directly from experimental results from the same set of samples. It is also a goal to develop improved calculation procedures so that the confidence in the numerical results is increased. It is shown that these goals are met by the developed procedure.

This relationship between the trapped charge and the potential barrier height involves several factors which might need to be modified. First, the dielectric constant in a heavily stressed, heavily damaged region near a grain boundary might be different than the accepted value for single crystal silicon. Unfortunately, no information is available concerning the dielectric constant under these circumstances. It is very difficult to independently measure the dielectric constant under any circumstances, and the permitivity is not well established as a function of doping even for single crystal silicon [30]. This is an example of a case where a single crystal parameter must be used because there is no other choice. Although it is not expected that the dielectric constant is largely different, the possiblility exists, and it would have a direct effect on the calculation of charge densities. In this study, the single crystal value of 11.8 e_o will be used. There are two other parameters in the charge density - barrier height equation which this study has investigated: the barrier height itself and the doping density.

In this study, the barrier height is a distributed variable rather than a constant. In the formulation of (5.1), the barrier height has been assumed to be the average or the uniform barrier in the material. Applying the previous distribution function developments, it is understood that now the barrier height functional must be integrated to arrive at the proper average for the trapped charge density. To perform the proper average, the expression (5.1) is integrated over the barrier height distribution function to get the average density of trapped charge. The program used to make this integration numerically on the Apple computer is given in the Appendix B, and essentially uses a modified Simpson's rule method. This case is an excellent example to illustrate how the distribution function can have a variable effect on the calculation, depending on the physics of the situation. Note that in this case, the weighting function has a square root dependence on the distributed variable, while the previous barrier height case had an exponential dependence. Thus, this case will have much less sensitivity to the nature of the distribution function. Indeed, in this case, the calculations have been performed with both procedures; integrating over the Gaussian distribution function and performing the classical calculation with the average from the distribution expression. Because of the very weak square root function, there was less than one percent difference in the calculated density of trapped charge between the two procedures. This indicates that the simple approximations are sometimes valid, but does not diminish the value of the distribution function procedure when the weighting functions are strong, such as the exponential and inverse function previously considered.

So far, two parameters have been studied where neither has been identified as serious problems in the current practice. The final parameter of this equation to be considered can have a sizable effect on the calculation of the trapped charge density at the grain boundary. This is the case of the effects of a profile in the dopant density near the grain boundary. In the formulation of (5.1), the dopant density is assumed to be constant throughout the bulk of each grain. At the same time, most reports accept the fact that dopant segregation occurs in phosphorus and arsenic doped polysilicon material [20,22,23,24]. When segregation occurs, this means that the density of phosphorus atoms at the grain boundary is larger than the density in the bulk of the grain. However, it is impossible to have an abrupt change from one density to the other when diffusion is allowed to occur. The diffusion equation [34] requires that aprofile exists where the dopant density varies smoothly from the large density at the grain boundary down to the constant level in the bulk of the grain. The diffusion equation has been solved by other authors for the case of polycrystalline materials [14,29,40,41], and this tendency is confirmed, although the exact solution depends on several choices of values of the appropriate diffusion constants. There still is much uncertainty about even the order of magnitudes of these various diffusion constants. The qualitative effects that any profile in the dopant density will have on the calculations of the charge density at the grain boundary will now be derived.

As discussed previously, Gauss's law relationships define the interaction of the depletion region at the grain boundary with the barrier height and trapped charge density. In deriving this relationship, the depletion charge is integrated to get both the potential barrier voltage and the total charge in the depletion region. The depletion charge is then assumed to be equal to the grain boundary charge from charge neutrality considerations. Since the depletion charge is obtained by integrating the dopant density, it is very important that the appropriate dopant density be used in this analysis, or errors will result. To show the qualitative effects of a nonuniform dopant density, this study will consider simple profiles, which will approximate the actual physical profiles for illustrative purposes. Most of these points can be made by considering a simple function, such as a quadratic, or even linear function. Since the exact variation is not known, and will vary from sample to sample, it is impractical to be more exact.

The main effect of the profile influence is exerted because the dopant profile will result in more ionized donors close to the grain boundary than the uniform approximation. Let us note that the barrier height is determined strictly from analysis of experimental results of the temperature dependence of resistance and does not depend on the assumed dopant density. To show the dopant profile effects, we must perform the derivation of (5.1) with the profile as the dopant density model. This is a simple Gauss's law calculation, as previously mentioned. The formulation for the charge density / barrier height relationship proceeds by the following integrations:

$$Q = 2\int_{0}^{W} N_d \, dx = 2 N_d W \qquad (5.2)$$

$$V_d = \int_{0}^{W} E(x) \, dl \qquad (5.3)$$

$$E(x) = \int_{0}^{x} qN_d/e \, dx = q N_d x/e \qquad (5.4)$$

$$V_d = \int_{0}^{W} q N_d x/e \, dx = W^2 q N_d/2e \qquad (5.5)$$

and substituting from the first integration yields

$$V_d = q N_d/2e \, (Q/2N_d)^2 = q Q^2/8eN_d \qquad (5.6)$$

This is the formulation when the doping density is assumed constant, and the outline of the procedure when the profile is general. It is noted that the $1/N_d$ dependence of barrier height in the classical model [5,16] can be explicitly derived. From the paper by Gilmer and Farrell[29], it is seen that assumptions must be made in calculating the solution to the diffusion equation, and the profile at the boundary will depend on these assumptions. However, it is noted that in many cases, a constant in the grain bulk with an approximately linear approach to the grain boundary is seen. A further assumption, concerning the depletion width, must be made since the integration dx is carried out over this distance. One would not expect that the diffusion profile extent would exactly correspond to the depletion width: indeed, when the barrier heights vary it would be impossible to always have this condition. However, this is the assumption which must be made, to simplify the integration. The results will indicate the trend, and further analysis directions will be clear. Much better integration procedure could be implemented with more complicated computer code. Assuming this linear profile, and changing the integration over distance around gives

$$N_d(0) = N_{do} = \text{bulk value} \tag{5.7}$$

$$N_d(W) = N_{do}(A + 1) = \text{boundary value} \tag{5.8}$$

$$N_d(x) = N_{do}(1 + Ax/W) \tag{5.9}$$

$$Q = 2 N_{do}W (1 + A/2) \tag{5.10}$$

$$E(x) = qN_{do}/e (x + Ax^2/2W) \tag{5.11}$$

$$V_d = q N_{do}W^2/2e (1 + A/3) \tag{5.12}$$

$$V_d = q Q^2/8eN_{do} (1 + A/3)/(1 + A/2)^2 \tag{5.13}$$

Now we can see the effects of the profile since the final expression is the original result times the factor including the profile parameter A. It is seen that the assymptotic behavior of the added expression approaches 1/A as A increases. The factor will always be less than 1, meaning that there will always be more charge at the grain boundary than in the constant doping case, as long as the profile increases toward the boundary. The qualitative result is that the constant 8 in the classical equation is replaced by a variable which depends on the profile assumed, but is always larger as long as the dopant density at the grain boundary is more than the bulk density. This means that the effect of dopant segregation is to increase the estimate of the trapped charge density at the grain boundary. It is noted that a new interaction has been discovered: inclusion of the effects of segregation now implies a stronger effect of carrier trapping. This is the first report that the two mechanisms are intimately interrelated, although it has been expected that both mechanisms are active in this material. Note that a more severe profile (steeper) will result in more effect, and thus more charge at the grain boundary for the same barrier height. The barrier height is not affected by the dopant profile since this parameter is extracted from the temperature data and the thermionic emission model does not involve the details of the depletion region. A couple of further comments are in order. First, it was unrealistic to assume that the depletion region and the diffusion profile have the same edge. Also, care must be taken with the assignment of the bulk of the grain, uniform value of the dopant density because the assumed profile contains part of the implant dose and thus reduces the dose involved in the uniform portion of the profile. How much of a difference this can make depends on the spatial extent of the profile into the grain as a percentage of the total grain. Independent of these slight concerns, the qualitative effects derived still hold; the segregation model increases the calculated density of trapped charge.

It has just been shown that the mechanism of dopant segregation suggests that a profile might exist in the dopant density near the grain boundary. This has been shown to increase the estimate of the trapped charge density at the grain boundary. The remainder of the procedure for the majority carrier census will now be discussed.

The relationship just investigated has as its result the areal density of trapped charge at the grain boundary. To express this result as a volume density, the areal density must be multiplied by the surface-to-volume ratio for that material. This parameter has also been addressed by this study, with the values being determined directly from the results of the TEM experiment. This product gives the volume density of charge trapped in the polysilicon material. These values are presented in Table 7.2, and will be discussed in detail in the next chapter. Due to the uncertainty in assigning the average barrier height to the infinite temperature term, these calculations have been performed for the average barrier obtained by the Gaussian model, for the room temperature value assuming the Taylor series definitions, and for the cases of with and without the profile effect. The trapped charge density is added to the free carrier density determined by the Hall effect to arrive at the total carrier density in the material. This total density is also the net density of ionized donors in the material. Since we know the implanted dose, we can calculate the total density of missing donors; the amount that can be attributed to segregation. As has been mentioned, the outcome of this calculation for our samples indicates that a large majority of the carriers are accounted for by this procedure. This is the case even without the increase caused by the inclusion of the profile effects, that is, no profile must be assumed to get this result. Segregation is still an observed phenomenon, and these results cannot change this fact. Rather, these indications suggest that the assumption that the segregated donors are inactive might be in question, or that some other oversight has occurred. As we have seen, every assumption can affect the outcome of these calculations, and this is the reason for doing the calculations.

In summary, the calculation procedures for the majority carrier census have been described. It is seen that the various charge subsets can be derived strictly from the experimental results. It is also seen that the formulae used to make these calculations involve assumptions about the properties of the material and local properties, and that these assumptions must be carefully chosen. The models presented include three effects which tend to increase the estimate of the charge trapped at grain boundaries:

1. The profile of dopant which must exist if dopant segregation occurs will require more charge to be stored at the boundary, relative to the approximation that the dopant density is uniform.

2. The proper calculation of the total boundary surface area will result in a larger area and thus more charge storage, due to the influence of the small grains. This calculation is performed using the observed grain size distribution function, rather than the average grain size.

3. The model for the temperature variation, which is described in another section, produces barrier heights slightly larger than those resulting from previous calculations, and this in turn indicates more charge is stored at the grain boundaries.

Each of these effects has been described, and the calculation procedure derived. It has been shown that the procedure gives reasonable results that lead to the conclusion that dopant segregation is not required to explain the charge distribution in this material.

CHAPTER VI

EXPERIMENTAL DETAILS

In this chapter, the details of the experimental device fabrication process, the measurement techniques, and the analysis procedures will be presented. One of the goals of this study is to determine all the necessary information for the the resistivity model directly from experimental results, and this process will be explained.

The first area of discussion is the device structure. This study uses devices which are quite simple to fabricate by integrated circuit standards. The starting material is a silicon wafer, which is then oxidized thermally to a thickness of 1000 A. The starting wafers for this investigation were three inch, 3 - 5 ohm cm phosphorus doped (100) slices. After oxidation, the polysilicon deposit follows, and is performed by standard LPCVD deposition. The material is then implanted with phosphorus at 100keV to the various doses determined by the experiment plan. These doses varied from 10^{14} to 10^{16} ions per square centimeter in the runs for this study. Next, the polysilicon is patterned into the rectangular structures with the 765 mask set. The implant anneal came next, and was performed at temperatures from 900 to 1200 ^{o}C, for 20 minutes. The structures are now covered with CVD silicon dioxide as a passivation. Contact apertures are patterned and opened, and the contact phosphorus deposit is performed. This contact deposit is required to insure that a good ohmic contact to the polysilicon is obtained. It is noted that this cycle is the dominant high temperature cycle for the control samples, those which did not receive any other anneal treatment. Now the aluminum metallization is electron beam evaporated onto the wafer, to a thickness of about one micron, and patterned to the interconnect pattern of the proper 765 mask. Finally, a contact sinter in forming gas is performed to further insure the ohmic contact. It is noted that the slices also receive a backlap and backside gold process to provide ease of packaging.

The devices are now ready for testing. First, the appropriate dice are selected, since there are four repeated patterns in this mask set, andthe dice are packaged and the selected structures bonded out. The packages used by this study included a standard military ceramic dual-inline-package (DIP) and a nonstandard, nonmagnetic ceramic DIP. The nonmagnetic package was required for Hall Effect measurement, but was difficult for the Harris people to obtain, and thus not all slices were available in the nonmagnetic packages.

6.1: Electrical Measurement Techniques

The electrical testing proceedures will be described next. The primary device to be tested was a simple van der Pauw structure consisting of a square of polysilicon one millimeter on a side, with four contact regions along the periphery. The measurement to obtain the sheet resistance required that a current be passed through two adjacent contacts while the voltage difference is monitored at the other two contacts. The sheet resistance is then determined as a constant times the ratio of the voltage to the current. This measurement was performed at the University of Florida using standard bench current source and digital voltmeter and at Harris using a LOMAC automatic tester. At the university, the measurements were performed over a temperature range of 77-350 $^{\circ}$K while at Harris the temperature range available was 225-425 $^{\circ}$K. It is noted that the measurements were performed with all four possible combinations of voltage and current directions and the results averaged. Also, at least five devices from each slice were measured to determine the average resistance function for that slice. The Hall measurement technique is quite similar and uses the same device structure. The additional equipment needed beyond the resistivity measurement is just a controlled magnet, in this case the Varian electromagnet at the University of Florida. For this measurement, the device is placed in a magnetic field which is normal to the plane of the wafer and a current is passed between two opposite contacts on the device. The Hall voltage appears across the other two terminals, and is the result of the interaction between the moving carriers of the current and the magnetic field. Note that there should be no Hall voltage when there is no field applied, and the magnitude of the stray voltage present in some devices impacts the accuracy of the Hall measurement. Again, the measurements are performed with both possible combinations of contacts, and also with the current and the magnetic field reversed, and the results are averaged. The Hall measurements are also taken as a function of temperature over the range 77-350 ^{o}K.

Some additional characterization was performed by taking the current- voltage relationship of some rectangular resistorsin an attempt to obtain the grain size from electrical measurements. These experiments were also quite simple, since it just involved semiautomatic procedures on an advanced Hewlett-Packard picoammeter. As will be seen, these measurements did not produce good results.

Finally, the last electrical measurements were for the capacitance properties of this material. These measurements consisted of mainly capacitance versus voltage (C-V) and capacitance and resistance versus frequency. The C-V measurements were taken in Gainesville on the PAR 410 C-V plotter, on simple MOS capacitors where the semiconductor material was the polysilicon under study. The capacitance versus frequency measurements were performed at Harris using a Hewlett-Packard 4175A Inductance-Capacitance-Resistance meter.

6.2: Transmission Electron Microscope Technique

The Transmission Electron Microscope is an analytic instrument with capabilities that can give significant information to the study of the microstructure of polysilicon. The name of this instrument identifies its function; it forms images from the transmission of electrons through the material under study. This provides the possibility to analyze material by the diffraction of this electron beam with the crystal structure of the material under study. Since very fine beams of electrons can be manipulated with great accuracy, this instrument has extremely good resolution, on the order of 10 Å. The instrument has a very sensitive sample stage, so that the orientation relative to the beam can be adjusted with great precision. This particular instrument has a high voltage level of 200keV, which determines the depth through which the electrons can travel, and thus the maximum sample thickness. The combination of these properties is such that the crystal structure of these thin-films of polysilicon can be studied with extreme precision. A film of polysilicon will image the different grains in contrast as the various grain's lattices diffract at different angles to the incoming beam. This is the primary TEM technique used in this study; investigation of the grain structure by using diffraction contrast and very high magnification. Most of the work of this study was done in bright field contrast at a magnification of 100kX.

A major part of any TEM study is sample preparation. The physical structure of the microscope requires that a sample 3mm in diameter be provided with the material to be studied supported and yet less than one micron thick. The layers less than one micron thick are very delicate, and must be carefully handled. Many samples must be attempted before good results can be reliably obtained. However, good results can be obtained by careful application of good technique and much practice. Fortunately, in the world of silicon processing, there is much history to draw upon for sample preparation. This study developed procedures which consist of wet chemical processing. This was found to be adequate though not optimum. The polysilicon to be studied is deposited on thermal oxide and then covered with deposited oxide and metallization. Initial attempts to float the polysilicon off the oxide by dissolving all the oxide in an HF etch were unsuccessful. It was found that the oxide etch would not undercut the polysilicon enough to get a supportable sample. Other frontside etch attempts were also unsuccessful. It was found that a silicon etch from the back of the wafer would provide a good sample with a high yield (50%). The following is the process flow for my sample preparation.

1. Select a die from quadrant one of the 765 test mask. This section is chosen because it gives a large target area of polysilicon sheet film in about the center of the die. This is the van der Pauw structure which is also used in the electrical portion of the current study.

2. Mount the die top down onto a glass slide in black wax (Apeizon). This is accomplished by melting the wax in a bunsen burner and then placing the die face down in the soft wax. The wax must be soft enough to encroach entirely over the die except for a small hole in the center of the die about one third of the die area. The wax is then allowed to harden by cooling. This effectively forms an etch mask for the sample since the hole left exposes the intended area to the upcoming acid etch. As usual, the accuracy in masking determines the quality of the device fabrication. Note that the back of the wafer has been coated with gold, so a gold surface is now exposed.

3. Etch the gold with gold etch, aqua regia, full strength. The mask pattern is transferred to the gold layer by a one minute etch in aqua regia. The black wax is not noticeably affected by the

acid etch. Now the gold layer will act as the etch mask for the silicon etch.

4. Etch the silicon all the way through. The circular etch area is etched by a strong acid solution isotropically through the entire thickness of the silicon wafer. The etch solution is the classic combination of nitric and hydroflouric acids, mixed about six to one in this case. This was diluted with water for a slower solution for use near the end of the etch. This full strength solution will etch through the entire wafer in about 30 minutes. It also etches horizontally in the silicon at about the same rate, and thus undercuts the gold by the thickness of the wafer, about 12 mils. It is noted that the acid also attacks the black wax at a much higher rate. Thus, the gold mask is the layer which prevents the entire silicon surface from being consumed by the silicon etch. The wafer area protected by the gold mask forms a supporting ring which gives mechanical support to the sample area in the center of the die. The etch is watched, especially near the endpoint, and continues until the metallization pattern is visible; a clear sign that the silicon has been etched entirely through. The etch for silicon has little selectivity over oxide since it contains the oxide etch, HF. Thus the etch continues through the surface oxide and poly layers, and would consume the entire sample if not stopped. If the etch is stopped when it first clears the surface, there is a good chance that a good sample will result. It is noted that the silicon etch also attacks the glass slide onto which the sample is

attached. The area of glass exposed is minimized to conserve the silicon etch consistency.

5. The die is now removed from the glass slide. This is done by immersing the glass slide in tetrachloroethylene, TCE. After about ten minutes, the die will have been released by the undercut of the wax by the solvent. The die can now be examined under the microscope to determine whether the process has been successful in providing an etched edge where the polysilicon material is on the edge. Samples which are successful to this point are continued to completion.

6. The next step is another gold etch. By this time the gold is loosely attached in some areas and still tightly held in others. It can serve no more useful function and gets in the way if left on during TEM. It is removed by another few minutes in the aqua regia. This step also removes the aluminum metallization from the frontside of the die. This aluminization also interferes with TEM observation, and so must be removed. It takes longer in the aqua regia to remove the aluminum than the gold, so this is the process limiting factor at this step.

7. The final step in the sample preparation is another oxide etch. The sample at this step consists of a single die with a hole in the middle which has an etch edge exposing the polysilicon area. The backside etch does not undercut the frontside oxide, so the edge consists of oxide in most areas. This oxide is etched back with a very dilute HF solution for about one minute. Hopefully the polysilicon has now been etched from the top and the back to create

a knife's edge of polysilicon material exposed. It is found that the procedure works adquately well.

The sample is taken to the TEM room and cleaned a final time with freon before being placed in the microscope. It is then placed in a special sample holder that is designed to be rotated through 2 axes while in the microscope. This holder has a 3mm circular slot to accept samples. Fortunately, the die size of the 765 mask series has a 100 mil side, meaning that the diagonal is 141 mils, or just a little more than the 3 mm. By delicately fracturing off one corner of the sample, the sample is reduced in size just enough to fit in the slot, be held by the clip, and still provide the mechanical support of the remaining silicon wafer. The sample is now ready to be placed in the microscope. Basically the process is now to put the sample into the chamber so that the thin region of polysilicon is in the beam. The sample holder has micromanipulators controlled from the outside so that it can be positioned with extreme accuracy. When a good area is found, the beam adjustments are made so that focus is obtained and the proper exposure of the photographic film is possible. It is noted that much technique or much preserverence is required to achieve focus under arbitrary circumstances. The images obtained consist of the various grains shown clearly by diffraction contrast, each grain has a shade of gray corresponding to the angle between the beam and its crystal structure. Also, any crystallographic features of the material will also create their own forms of contrast and thus be visible in the images. The classic case is the dislocation which appears as a line in the TEM images. Also apparent are stacking faults, twins, shape contrast, etc. The interpretation of these images is a large measure of the techniques of TEM microscopy. It is also common to observe silicon dioxide and the single crystal silicon wafer from various areas of these images. Another imaging possibility is the diffraction pattern. In this case, the image does not correspond to the spatial property of the material, but rather is the diffracting beams themselves. This image provides the user with explicit information of the crystal structure. In our case this process can distinctly differentiate between the silicon wafer, the polysilicon, and the oxide. It is clear that even the different polysilicon samples can be related to their diffraction patterns, since the larger grain material gives brighter spots and less spots, than the fine grain material. Examples of TEM images and discussion will be forthcoming in chapter seven.

6.3: Analysis Procedures

The last part of the experimental details include a description of the anaylsis procedures used by this investigation. These procedures are designed to provide the parameters of the model which has been developed for the materials under study. The parameters which must be determined are the barrier height distribution function average and standard deviation, the surface-to-volume ratio, the carrier density, the resistivity prefactor and the results of the majority carrier census. These will each be described.

The barrier height distribution function parameters are determined from the experiment results of resistivity versus temperature. A computer program has been developed (see appendix A) which calculates these parameters directly from the input data of resistivity versus temperature. This program essentially just removes the linear dependence of the prefactor and then fits the remaining information with a least square regression formula. This function has been implemented in general form, where the statistics can include any number of terms, but it was found that the best results were obtained with just the barrier height and standard deviation as parameters. Note that this program also includes the 1.5 V_t correction term which came from the derivative of the Fermi level.

The Hall Effect experiment is quite simple in nature. The carrier density is determined directly by a constant to the voltage output of the experiment. The only complication is that the Hall factor r_H must be corrected for heavily doped samples. This work uses the Hall factor of 0.9 for all samples exhibiting a carrier density in excess of 10^{19} cm^{-3}.

The surface-to-volume ratio is determined directly from the TEM images obtained for the various polysilicon samples. Representative material was studied under the microscope and at least ten images of good quality were obtained for each process under consideration. Since each image shows many grains, this sample size provided at least one hundred grains for measurement. The procedure used to obtain the surface-to-volume ratio was to measure the area and perimeter of the image of each grain. The ratio of the perimeter to area is the estimate of the surface-to-volume ratio. Note that this requires the assumption that the ratio in two dimensions is a good estimate of the ratio is three dimensions, but since only two dimensional images are available, this was considered adequate. The measurement of the grain area was performed with good precision by using a planimeter, while the perimeter was measured with a flexible ruler. It is believed that this procedure provided a good evaluation of the surface-to-volume ratio.

When all the preceding parameters have been evaluated, it is finally necessary to fit the functional to the observed data. This step determines the final prefactor, and is evaluated at the room temperature data point in this study. This final factor is approximately equivalent to the Richardson constant except that the constant in this case is dependent on the material properties and thus varies from sample to sample. It was hoped that a universal constant could be obtained at this step, but the results clearly show that orders of magnitude differences occur in the results for the various process materials.

The final procedure to be discussed is the majority carrier census. This procedure was discussed in detail in the preceding chapter. The method essentially counts the carriers at each location in the material to arrive at the distribution among the various subsets. The trapped charge density is evaluated by computer integration over the distribution function for barrier heights which is determined from the resistivity function of temperature. The program used to calculate this charge set is shown in Appendix B and uses the Simpson's rule method to calculate the integral. Note that the equation for this integration will use the results of the dopant profile analysis in the appropriate cases. This results in the average areal density of charge at the grain boundaries in the specific material associated with the distribution function parameters input. The volume density of trapped charge is obtained by multiplying the areal density by the surface-to-volume ratio. This is added to the Hall carrier density to get the total density of majority charge in the material. The difference between the resulting total density of majority carriers and the implant dose is our estimate of the dopant segregation, which will be negative in some cases. This is the procedure of the majority carrier census.

In summary, this chapter has presented the details of the experimental procedures utilized in this study. These procedures include device fabrication, electrical measurements, transmission electron microscopy, and mathematical analysis. The results of these procdures will be shown in the next chapter.

CHAPTER VII

RESULTS AND DISCUSSION

In this section the presentation of the results of the experimental measurements and the calculation of all the model parameters for the polysilicon samples is made. The primary measurements included resistivity versus temperature, Hall Effect versus temperature, and transmission electron microscope imaging. These tests were performed on the LPCVD polysilicon resistors fabricated with standard IC processes by Harris Semiconductor. The characteristics will be generally reported by run and slice number with the processes for each slice described in Table 7.1.

The first experiment to be discussed is the resistivity versus temperature experiment where it is expected to see a curving Arrhenius plot, as described in Chapter IV. As seen in Figures 7.1 - 7.10, most results are quite as predicted with the curvature and slope of the resistivity function being dependent on the various process conditions. The lightly doped samples have much steeper slopes and correspondingly high barrier heights. They also have a greater curvature indicating a larger variation in the barrier heights as described by the standard deviation. In this section, the detailed characteristics of these devices determined by experiment will be discussed along with a presentation of the model calculations.

Table 7.1

Process Conditions for Runs CR-1, CR-2 and CR-3

Slice Number	Implant Dose 10^{14} cm^{-2}	Anneal Temperature °C
CR-1 AND CR-2		
43	1	none
44	10	none
45	100	none
48	1	900
49	10	900
50	100	900
53	1	1000
54	10	1000
55	100	1000
58	1	1100
59	10	1100
60	100	1100
63	1	H_2
64	10	H_2
65	100	H_2
68	1	900 + H_2
69	10	900 + H_2
70	100	900 + H_2
73	1	1100 + H_2
74	10	1100 + H_2
75	100	1100 + H_2
78	1	1200 prebake
79	10	1200 prebake
80	100	1200 prebake
CR-3		
1-5	2.5	1100
6-10	5.0	1100
11-15	7.5	1100
16-20	10	1100
21-25	25	1100
26-30	50	1100
31-35	75	1100
36-40	100	1100
41-45	2.5	1200
46-50	5.0	1200
51-55	7.5	1200
56-60	10	1200

7.1:Runs CR-1 and CR-2

The first group of samples to be discussed are runs CR-1 and CR-2. These runs are discussed together since they both received the same processes, and were run by exactly the same recipe. The run CR-2 was designed to be the backup for CR-1, and this turned out to be a fortunate plan since half the run CR-1 was ruined in process. The variables covered by these runs included implant over the range between 10^{12} to 10^{16} cm^{-2} and anneals from none to 1200 ^{o}C. The devices which received implants of less than 10^{14} cm^{-2} were too resistive to measure accurately with the equipment available. Also, these runs included experiments to try hydrogen anneals at 450 ^{o}C, and these will be discussed separately. The processes for these samples are indicated in the Table 7.1.

Slices 43,48,53,73:

The first group of slices to be discussed received the lowest implant dose; 10^{14} cm^{-2}. These devices have very high resistance and high barrier height. They also have an interesting and somewhat surprising functional dependence on the anneal temperature. The control slice of this group, slice 43, received no implant anneal except for the contact predep. This slice shows a sheet resistance which varies over temperature between 500k and 50M ohms per square, see Figure 7.1, with a barrier height average of 0.432, a sigma of 0.073, and a room temperature barrier of 0.328. These results would be considered typical for the reports in the literature, since the barrier height of 0.55eV, or one half the energy gap of silicon is the standard result for low doped devices. It is also noted that the

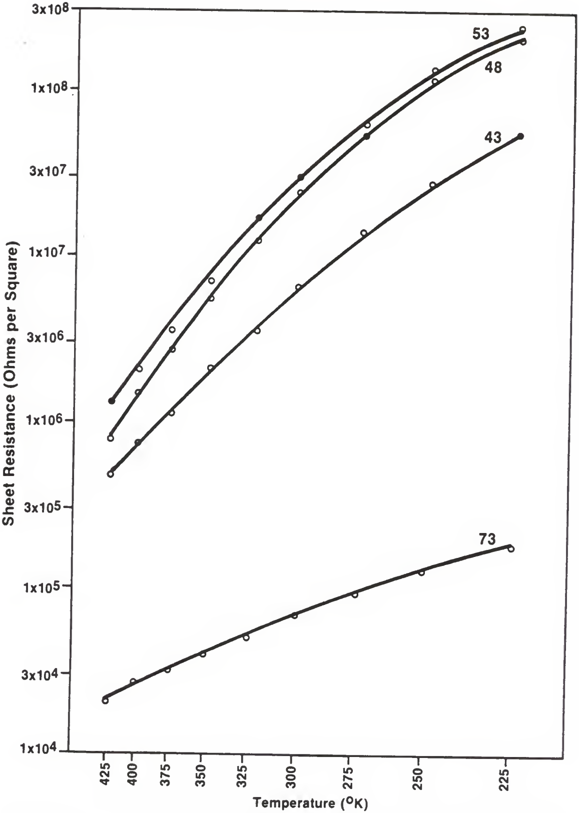


Figure 7.1: Sheet resistance versus temperature for slices from runs CR-1 and CR-2 which received an implant dose of 10^{14} cm^{-2}.

"control" group was the least controlled, i.e., they had the most variation within the wafer, and this was quite significant. At the lowest temperatures, the devices of this wafer varied by more than an order of magnitude. The next entry in the sequence, the slice 48, which received the 900 °C anneal, actually exhibits higher resistance and larger barrier height, seemingly in contradiction to accepted trends, although there has been reports of this trend in the literature [11]. The sheet resistance of this wafer was about twice the control slice average, varying between 800k to 200M ohms per square. The barrier characteristics are average 0.707, sigma 0.107, and the room temperature barrier was 0.485; all the barrier statistics are shown in Table 7.2. Note that even the standard deviation increases relative to the control slice, indicating that this anneal is more nonuniform than the split that received no anneal. This does not tell the whole story, however, since the reproducability, as indicated by the variation between die from the same wafer, was much better for 48 than for 43. Also notice that the room temperature barrier height of 0.485 still corresponds closely to the literature reports of one half the bandgap for lightly doped polysilicon. The next element in this series, slice 53, received a 1000 °C anneal, and continues the trend to higher sheet resistance, although the barrier height is slightly less. It is seen that 53 and 48 have very close characteristics, with 53 having slightly less slope, reflected in its barrier parameters; average barrier 0.693, sigma of 0.107, and room temperature barrier of 0.471. Again, it should be pointed out that the these resistors are very similar to

Table 7.2

Model Parameter Results for CR-1 and CR-2

slice	$\langle V_d \rangle$ volt	sigma volt	Ea(RT) volt	R_o ohm-cm	S_v 10^5 cm^{-1}
43	.432	.073	.328	20.7	5.73
48	.707	.107	.485	.183	5.10
53	.693	.107	.471	.402	4.06
73	.226	.053	.171	97.7	2.45
78	.079	.020	.070	277.7	2.03
44	.065	.022	.055	112.7	5.61
49	.072	.025	.059	103.8	4.91
54	.060	.021	.051	106.3	3.82
74	.046	.015	.041	68.9	2.04

slice	N 10^{17} cm^{-3}	N_t 10^{12}cm^{-2}	N_t 10^{17}cm^{-3}	N_{TOTAL} 10^{18}cm^{-3}	IMPLANT 10^{18}cm^{-3}
43	4.1	5.82	32.7	3.68	2.0
48	4.4	7.08	34.7	3.91	2.0
53	4.8	6.97	26.6	3.14	2.0
73	8.1	4.20	8.57	1.67	2.0
78	16.0	2.69	5.46	2.15	2.0
44	52.0	7.51	42.1	12.3	20.0
49	73.1	7.80	38.3	11.1	20.0
54	63.7	7.22	27.6	9.13	20.0
74	107	6.48	13.2	12.0	20.0

slice	N_{tmax} 10^{12} cm^{-2}	N_{tmax} 10^{17}cm^{-3}	N_{TOTmax} 10^{17}cm^{-3}	IMPLANT 10^{17}cm^{-3}
43	10.0	57.4	61.5	20
48	12.8	65.4	69.8	20
53	12.7	51.5	56.3	20
73	7.24	17.7	25.8	20
78	4.29	8.70	24.7	20
44	12.2	68.7	120.7	200
49	12.9	63.4	136.6	200
54	11.7	44.9	108.6	200
74	10.3	21.0	128.0	200

slice 48, although the higher temperature anneal was used, and this is indicated by the equality in the standard deviation.

The next elements in this sequence are devices with more desirable characteristics, namely lower barrier height. This is seen starting with slice 73, which received the 1100 °C anneal plus a hydrogen anneal. (No wafer with 1100 °C anneal only at this implant survived the fabrication sequence, this would have been slice 58). The step from 1000 °C to 1100 °C anneal makes a big difference, with two orders of magnitude drop in resistance and correspondingly large drop in the barrier and sigma. It is thought that this drastic change is generated by grain growth in the polysilicon, and there have been reports that this occurs between 1000 °C and 1100 °C [11,42]. At this implant dose, even the 1100 °C samples have a high sheet resistance 10k to 100k ohms per square, but the drop with this anneal is clearly central to achieving the characteristics desired. Also, this anneal produces the most consistency between samples of the same wafer, with all devices having values within about 5% of the norm. The barrier characteristics are average 0.226, sigma 0.053, and room temperature barrier of 0.171. The final element in this sequence is slice 78 which received a 1200 °C anneal before implant and only the predep furnace treatment after implant. Its characteristics show resistance which is another order of magnitude lower that 73, with sheet resistance varying from 3k to 7k ohms per square. The slope is also very mild, with barrier parameters; average of 0.079, sigma of 0.020, and room temperature barrier of 0.070. With the standard deviation this low, the plot appears very close to the straight line anticipated for a zero standard deviation. The reduction of resistance is again attributed to grain growth, but this will be discussed in the section on TEM. In summary, the characteristics of this implant dose vary extremely between slices which received the various temperature treatments. Several trends are noted: first, for anneals of 1000 °C or less, the resistance increases, though the barrier parameters are not monotonic. This trend is attributed to dopant and carrier redistributions, where the tendency to trap dopants and carriers is increased when the dopants and carriers are allowed to diffuse to areas which are not saturated at the grain boundary. Finally, the 1100 and 1200 °C anneals greatly reduce the resistance and barriers due to the enhanced grain size after these anneals.

Next, the majority carrier census will be discussed for all the elements in this group. These results are also shown in Table 7.2. There are several cases indicated to discuss, the "normal" values which are calculated using the room temperature barrier height and the trapped charge formula without the segregation effect, and the maximum values which are calculated with the "average" barrier height and the profile effect on the trapped charge. The profile assumed for this calculation is a modest linear increase to a density at the boundary of twice the bulk grain value. This profile will increase the estimate of the trapped charge by 50%. First for the normal values, which are used to correspond to the values previously presented in the literature, it is seen as a general trend that the slices implanted at 10^{14} cm^{-2} have more than the implant dose of majority carriers indicated, by an amount which varies with the exact slice. Only the 1100 °C sample has less than the implant dose of majority charge shown. It is noted that the segregation effect predicted by the thermodynamic derivation suggests that less carriers will be trapped in the devices which received the higher temperature anneals, while the data presented here show the opposite effect, namely the increase in temperature shows less charge accounted, and thus would indicate more segregation effect at the higher temperatures. With the modifications which increase the estimates of the trapped charge, all samples in this group have much excess of charge indicated, and this suggests that the assumption that segregation of dopant removes its carrier contribution should be re-evaluated.

Slices 44,49,54,74

The next data collection to be described is the characteristics of sheet resistance for those wafers implanted to 10^{15}cm^{-2}. These data plots are shown in Figure 7.2. It is immediately noticed that the curves are much closer together, indicating that the characteristics are not nearly so sensitive to anneal as are the lower dose implants. Also, the lines are much straighter, coming close to the classical straight line of thermionic emission. The control wafer for this group is slice 44, with sheet resistance which varies from 700 to 1200 ohms per square. Its barrier characteristics include average 0.065, sigma of 0.022, and a room temperature barrier of 0.055. This standard deviation is as good as the best slices, 78 of the previous group. At this implant dose, the other problem of reproducability is also sharply reduced, giving

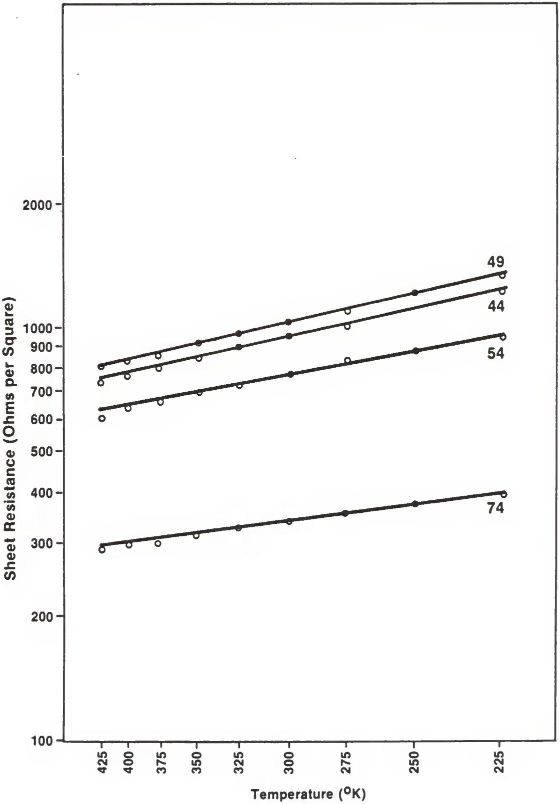


Figure 7.2: Sheet resistance versus temperature for slices from runs CR-1 and CR-2 which received an implant dose of 10^{15} cm^{-2}.

further support to our claim that this effect is due to dopant or carrier redistribution, since the increased dose is more likely to satisfy the local boundary requirements without needing the diffusion aid. Next slice 49 is examined, which received the 900 ^{o}C anneal, and notice its sheet resistance is very close to that of 44, being slightly higher, and following the trend of the lower dose. Its barrier characteristics are also quite similar, with average of 0.072, sigma of 0.025 and room temperature barrier of 0.059. Since these two are so close, it is believed that the properties are controlled by implant dose much more than by the anneal temperature, at least until the substantial grain growth occurs. Next we examine slice 54, which received the 1000 ^{o}C anneal. Its resistance is slightly lower than the previous three, with values between 600 and 1000 ohms per square. The fact that this slice has improved its relative position, that is, has lower resistance, suggests that the grain growth expected between 900 and 1000 ^{o}C, though less than at the next step, is enough to make the resistance less. The other effect, diffusion to available boundary states, has become less important since there are more dopants in all areas due to the higher implant. The barrier characteristics for slice 54 are average of 0.060, only slightly less than 44, sigma of 0.021, which is essentially the same as previous, and room temperature barrier of 0.051. The last slice, 59, is discussed next (no slice with the 1200 ^{o}C anneal at this implant dose made it through fabrication, it would have been slice 79). This slice 59 received the 1100 ^{o}C anneal. The sheet resistances vary between 270 and 400 ohms per square, with curves that appear quite straight. Again, the step between 1000 and 1100 °C results is a significant drop in resistance, much more than any other anneal step. The barrier characteristics are also quite mild, with the average being 0.047, sigma is 0.015, and the room temperature barrier is 0.042. Summarizing this implant dose, it is seen that the characteristics are much closer together, and much closer to classical models and desired properties. It is also noted that the higher anneal temperatures reduce the resistance by increasing the grain size and reducing the trap density, at anneals of 1000 °C or greater, with substantial improvement at 1100 °C. These are the devices closest to industrially useful for the desired application.

Finally, a discussion of the majority carrier census for these samples is in order. The results of these calculations is shown in Table 7.2. Again, the numbers are reported as the values which are calculated with the classical trapped charge formula and the room temperature barrier height, and then the increased estimates using the modified formula which includes a modest dopant profile and the average barrier height from the distribution function model. In this case it is seen that the lower values are less than the implant dose, by varying amounts in the range of 40–55%. This would be the predicted amount of segregation in the majority carrier census. Some comments on this point. First, the theory of dopant segregation predicts that less segregation occurs, as a percentage of the amount of dopant available, as the densities increase. However, the results of this study indicate that there is no room for segregation in the lower dose, and evidence of segregation in the higher dose, seemingly in contradiction to the theory. Also, the percentage of segregation should decrease as the anneal temperature is increased, but this is also contradicted except at the step from 1000 to 1100 °C. Also, it is noted that the inclusion of the new effects developed by this study, the larger average barrier and the effect of the profile, increases the estimate of the total majority charge density, reducing the estimated number of segregated dopant. In light of the undisputed electron microscope work that shows clearly the dopant atoms as being segregated, it is left that the assumption that these segregated atoms do not contribute to the majority charge must be questioned. Note that this result would have the boundary consisting of both the positively charged ionized donors and the negatively charged trapped carriers in some kind of matrix.

Slices 45,50,55,75,80

The last group of devices in this set are those that received the highest implant dose; 10^{16} cm^{-2}. The effective dopant density in this material is 2 10^{20} cm^{-3}. These devices show the sheet resistance versus temperature characteristics of Figure 7.3. These samples are very heavily doped, and the sheet resistances are very small, of the order of 40 ohms per square and less. It is also noted that the temperature variation has reversed, now the devices become more resistant as the temperature is increased. This means that the thermionic emission process has lost its dominance, and normal, ohmic conduction is prevailing. Thus, no barrier statistics will be presented for these devices. There is information available

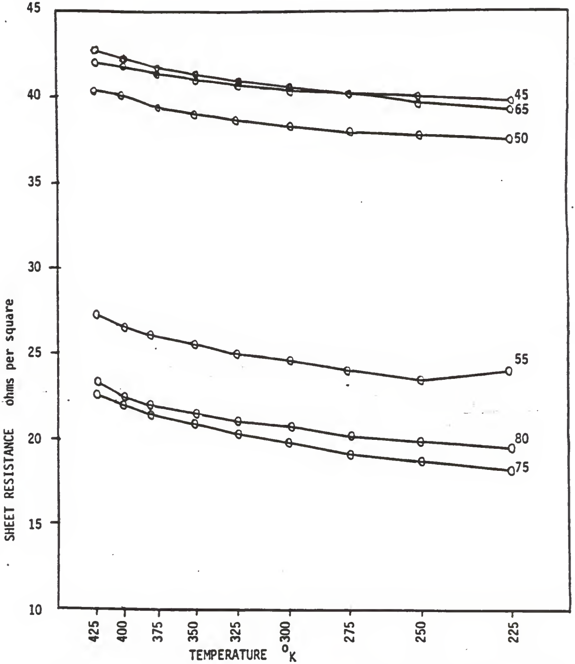


Figure 7.3: Sheet resistance versus temperature as a function of anneal temperature. These samples all received an implant dose of $10^{16} cm^{-2}$, and are from runs CR-1 and CR-2.

from these data, and it concerns the further trends due to the process temperatures. The first thing to note is that the control wafer, slice 45, has finally placed itself at the highest resistance, which was expected all along. Its sheet resistance is about 40 ohms per square. Right on top of that curve is the results for slice 65, which received control plus the hydrogen anneal. This result shows about the same resistance with only slightly larger temperature variation. Next, also about 40 ohms per square, is slice 50, which received the 900 °C anneal. Its resistance is only a fraction lower that the control slice. There is quite a space before the next lower sheet resistance occurs, slice 55, at about 25 ohms per square. This wafer was annealed at 1000 °C and shows more temperature variation than the wafers annealed at 900 °C or less. Finally, the last two slices have about the same sheet resistance, and are slices 75 and 80, annealed at 1100 °C plus hydrogen and 1200 °C pre-implant, respectively. In this case, the 1200 °C sample has slightly higher resistance, with about the same temperature dependence. Both of these last two devices have sheet resistances around 20 ohms per square. Summarizing the information for the heavy doped samples, it is seen that the thermionic emission model has become invalid, due to the temperature reversal of the resistivity data. It is also noted that the resistance value has become a much more regular function of the anneal temperature, with declining resistance as anneal temperature increases. This information is analyzed with the following conclusions; the grain boundary barriers have been essentially eliminated by the Debye screening of the high implant dose, thus the thermionic emission model is no longer valid. Now, the resistance is governed by the grain size of the material, with larger grains producing lower resistance. Also, the higher anneal temperatures produce larger grains, and thus producing lower resistivities. This analysis holds except for the 1100 and 1200 °C anneals, where it would be predicted that the 1200 °C anneal would produce larger grains and thus lower resistance. This does not account for the doping dependence of the grain growth process, which could be different for the 1100 and 1200 °C samples, since the 1200 °C wafer was annealed prior to implant, and thus does not gain the heavy doping enhancement of grain growth. If this doping enhancement is large enough, the grains in the 1100 °C sample could be larger than the 1200 °C prebake sample, and thus the data fall into place. It is noted that even the 1000 °C sample shows indications of doping enhanced grain growth, since it has shifted toward the characteristics of the higher annealed samples, while at lower doses it was closer to the lower anneal temperature devices. These trends of grain size will be examined explicitly in the TEM section.

7.2: Run CR-3

Chronologically, the results of the first two runs were analyzed before the third run, CR-3, was started so that the next group of samples could be more assured of being successful. Since the first group had problems in the areas of wafers out and low implant doses, the run CR-3 was designed differently so as to provide more information. It was decided to concentrate on the area indicated by the previous run to be most likely to achieve the desired characteristics. The run CR-3 was 80 wafers processed together through polysilicon deposit, and then divided into three subgroups, CR-3A, CR-3B and CR-3C.

Cr-3A.

This group of wafers were processed somewhat differently than the previous groups, CR-1 and CR-2. The process for this run had all samples receiving the same anneal, but with different implant doses. The doses are now more closely spaced, with values at 1, 2.5, 5 and 7.5 per decade, so that the doping dependence can be investigated more closely. The range of implants included from 10^{14} to $10^{16}cm^{-2}$. The anneal temperatures for this run was 1100 °C, and was chosen based on the results of CR-1 and CR-2. The matrix of wafer process was different for this run also. Instead of running only one wafer per process split, this run included five wafers receiving identical processing. This allowed the investigation of the wafer to wafer variation within a single run, and guaranteed that no holes in the matrix would result like the previous case. The results of this run variation test were quite encouraging for this group, with uniformity of 5% over the five wafers. This is quite different from the results of CR-3B, as will be seen. The resistivity versus temperature curves for these slices are presented in Figure 7.4. Again, it is seen that the curves obey the expected form, namely nearly straight lines on the semilog plot. From this plot, it is easy to recognise that, as the implant dose increases, the slope of the curve and thus the barrier height decrease. All curves have only slight curvature, similar to the previous 1100 °C

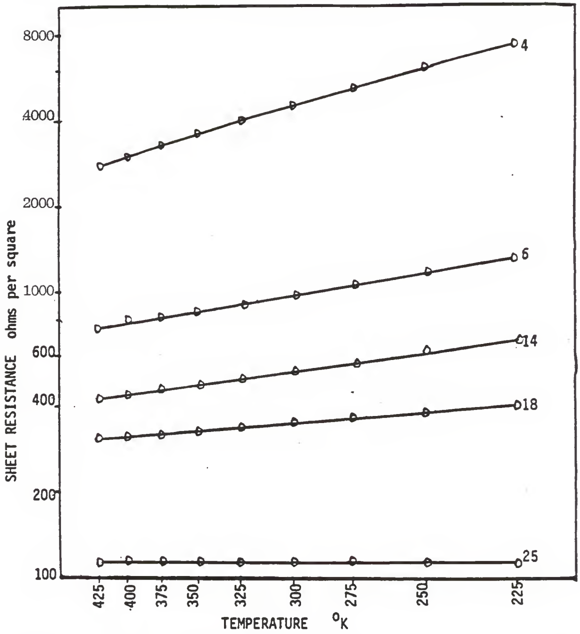


Figure 7.4: Sheet resistance versus temperature as a function of implant dose for run CR-3A. All samples were annealed at 1100 ^{o}C.

Table 7.3

Model Parameters for CR-3

slice	<Vd>	sigma	N
4	.120	.037	2.14e18
6	.091	.033	5.10e18
14	.081	.032	9.36e18
18	.075	.031	1.33e19
25			4.13e19
40,41,44	.095	.039	
45	.094	.038	
47,49	.080	.036	
50,51,52,53	.069	.033	
56,59	.063	.030	

samples, which coresponds to a low standard deviation. The barrier statistics follow a smooth trend from an average barrier of 0.120 for the wafer implanted at 2.5x10^{14}, with 0.091 for 5x10^{14}, 0.081 for 7.5x10^{14}, and 0.075 for 1x10^{15}. Notice from the figure that the curve for slice 25, implanted at 2.5x10^{15}, is a flat function of temperature, and thus no barrier stastics were determined. Since the previous slice has a measureable barrier, it might be wondered why the sudden drop. Actually, a barrier could be extracted from this device, since the additional correction terms would be offset by the barrier height and thus give a flat characteristic. The first correction is the T^1 dependence of the prefactor, which will contribute about 0.05eV to the barrier height. Also, the Fermi level correction term, which adds 1.5 V_t to the activation energy, adds the remainder to the extracted barrier height statistics. Thus, the flat resistance versus temperature characteristic actually requires a barrier of 0.06 to maintain its flat characteristic. This will be taken as the point where the model presented becomes invalid; theoretically, the barriers can be assumed to exist until they become as small as the order of kT, but practically, the flat resistance characteristic will be taken as the breakpoint of model validity. This is why the model was not applied in the previous case when the resistance curves declined rather than increasing. The other parameters of the model also behave smoothly, with sigma varying from 0.037 to 0.031 and the room temperature barrier height varying from 0.093 to 0.050. It is also noted that the correspondance between slice 18 of this run and slice 59 of CR-2B is very close, indicating that run to run uniformity is also good with the 1100 °C anneal. Overall, this process, 1100 °C anneal, gives the most consistent results of any devices tested.

CR-3B

This group of wafers was processed similarly to the previous group, with the exception that the common anneal temperature was 1200 °C rather than 1100 °C. Also, the range of implant densities was restricted to the 10^{14} to 10^{15} cm^{-2} range, since the previous results indicate that this is the range of practical interest. Again, five wafers of each implant dose were run together with identical process. The results for the resistivity versus temperature are shown if Figures 7.5 and 7.6. The results here are quite different from the previous case, since here the different wafers which were processed identically tend to have various characteristics. At each implant dose, there is a nominal characteristic, which usually about 50% or more of the devices come within about 5% of obeying. The other devices, those not nominal, tend to scatter over a wide range. Looking first at those implanted 2.5×10^{14} cm^{-2}, it is seen that all of slice 40 and 44 have very close properties, with sheet resistance between 1000 and 2000 ohms per square, and obeying the expected nearly straight line. Several devices from slice 41 also have this characteristic. The devices from slice 42, which was processed the same, have much lower resistance, 300 ohms per square, and nearly flat temperature dependence. Also, some devices showed very assymmetric characteristic, having much larger resistance in one direction than in the perpendicular direction. These results are interpreted by

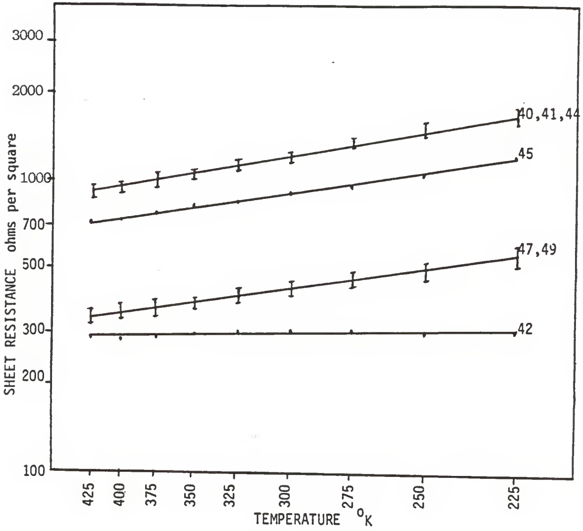


Figure 7.5: Sheet resistance versus temperature for slices from run CR-3B which all received an anneal at 1200 °C.

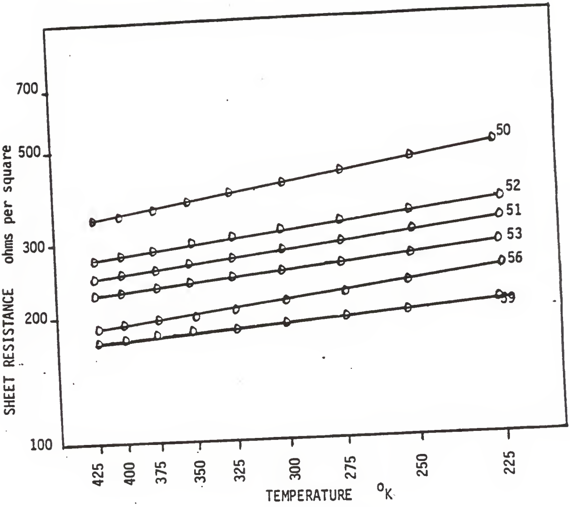


Figure 7.6: Sheet resistance versus temperature for slices from run CR-3B, which all received an anneal at 1200 °C.

anticipatingthat significant grain growth occurs between the 1100 and 1200 °C anneal processes. Since these samples were annealed at 1200 °C it is believed that the grain growth mechanism was very strong, and indeed created grains too large for uniform characteristics. Those devices obeying the nominal characteristic have an average distribution of grains, including some smaller grains, so that the terminal characteristics are similar to the average for this process. Those devices where the grains become extremely large, or where unusual arrangements of the larger grains occur, give the assymmetric and other unusual characteristics. These hypotheses will be reexamined when the TEM results are discussed. The barrier statistics are presented by wafer rather than average over all wafers the same, since the characteristics are so unpredictable. It is seen that those obeying the nominal characteristic have average barrier heights about 0.095, sigma of 0.039 and room temperature barrier of 0.073. The results for those slices implanted to 5×10^{14} cm^{-2} are similar as seen in Figure 7.5. In this case, much variation between slices whose process was the same is again observed. This time, the nominal characteristic is around 400 ohms per square with the usual temperature variation, average barrier about 0.080, sigma of 0.036, and room temperature barrier of 0.068. It is noted that even among those with the nominal characteristic, the temperature function is somewhat rough, or the data appears to scatter from the average line. The nominal slices include 47 and 49. Slice 45, processed the same, is consistently much higher in sheet resistance, with values between

700 and 1500 ohms per square, more than twice the nominal characteristics. The barrier statistics are also different, with values of average barrier 0.094, sigma of 0.038, and room temperature barrier of 0.086. Slice 45 would fit better into the previous group, just as slice 42 would be closer to this group. The explanations are the same, with the modification that the doping enhancement of grain growth can be causing the problem to be worse as the implant increases. The higher implant doses show the same kind of thing, though no slice is consistently out of range, there is a large band of characteristics where the individual die fall within. The barrier statistics at 7.5×10^{14} cm^{-2} are average barrier about 0.069, sigma about 0.033, and room temperature barrier about 0.057. For the implant dose of 10^{15} cm^{-2}, the situation is the same, with barrier statistics of average barrier about 0.063, sigma about 0.030, and room temperature barrier of 0.054. It is unfortunate that neither wafer no. 79 from CR-1B or CR-2B survived, since this would have allowed direct comparison of the effects of the 1200 °C anneal before and after implant. By comparing CR-3B with CR-3A it is seen that the 1200 °C anneal reduced the resistivity and the barrier height by a substantial amount, such that the resistance of the 1200 °C, 2.5×10^{14} cm^{-2} is similar to the 1100 °C 5×10^{14} cm^{-2} devices, and so forth. Summarizing, the 1200 °C anneal created very low resistance resistors with much scatter in the values die to die. It is believed that this temperature is too high to obtain useful material in a production environment. The discussion of the grain growth processes will be renewed in a later section.

7.3 Hydrogen Passivation Attempts

In this section, the effects of hydrogen passivation of the grain boundaries will be discussed. A very important aspect of recent reports in the literature on polysilicon is the prevalence of hydrogen treatments [43,44,45,46]. Universally, these reports indicate that the presence of hydrogen in polysilicon causes some kind of reaction such that the grain boundary states no longer trap charges. This is clearly the kind of effect desired, and these reports indicate significant improvement in the observed properties. This study also included experiments involving the hydrogen passivation of the grain boundaries. Each wafer lot included some slices dedicated to this experiment. The bad news is simply that the reports of the literature were not reproduced. No treatments attempted by this study resulted in improved properties. These experiments will now be discussed.

The hydrogen process can be performed in several ways [43,44,45]. The process attempted in runs CR-1 and CR-2 was a hydrogen gas anneal in the range of 450 °C. In this process, the wafers are simply placed in a furnace tube in the hydrogen ambient. It has been reported in the literature [43] that this would passivate the boundaries, although not all reports agree on this point. The results of this study indicate very weak influence and the trend is to make the resistance higher, not lower, see Figure 7.7. In our case this can be explained by a process error, since the wafers must not see any temperatures greater than 500 °C after the hydrogen treatment, but the traveler was written so that the

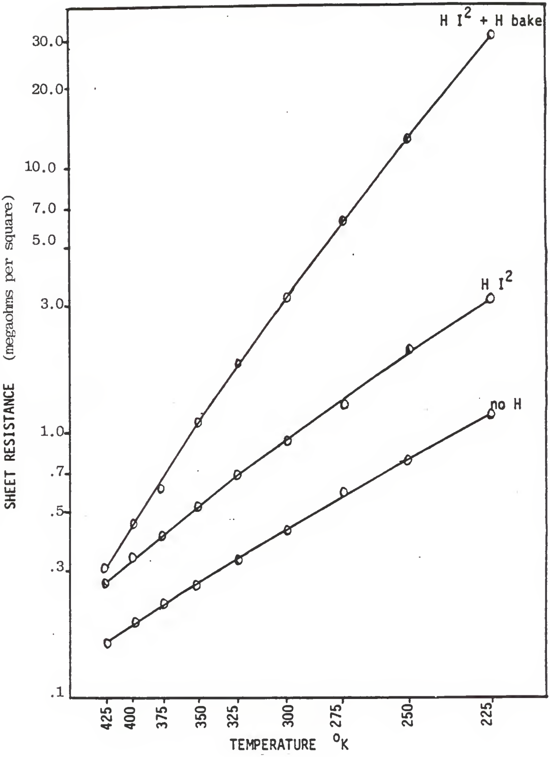


Figure 7.7: Sheet resistance versus temperature for slices from run CR-3C which received an implant dose of 10^{14} cm^{-2} and a hydrogen implant.

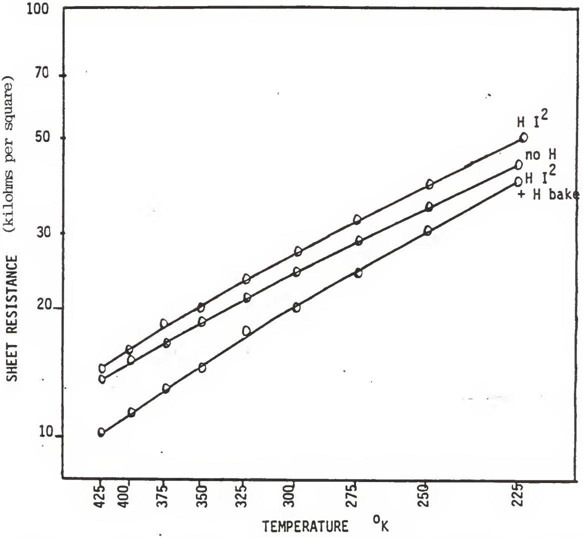


Figure 7.8: Sheet resistance versus temperature for slices from run CR-3C which received an implant dose of $2.5x10^{14}$ cm^{-2} and a hydrogen implant.

Table 7.4

Results of Run CR-4

SLICE	P IMPLANT 10^{14}CM^{-2}	ANNEAL TEMP ^{O}C	H IMPLANT 10^{13}CM^{-2}	SINTER TEMP, GAS ^{O}C	SHEET RESISTANCE KOHMS/SQUARE
1	2.5	950	none	450 N_2	163
2	2.5	950	none	450 H_2N_2	154
3	2.5	950	none	450 H_2	2180
4	2.5	950	3	350 N_2	454
5	2.5	950	3	450 N_2	517
6	2.5	950	3	350 H_2N_2	299
7	2.5	950	3	450 H_2N_2	468
8	2.5	950	3	410 N_2	350
10	2.5	950	100	350 N_2	90
11	2.5	950	100	450 N_2	185
13	2.5	950	100	450 H_2N_2	269
14	2.5	950	100	410 N_2	121
15	2.5	950	100	450 N_2	1150
16	2.5	1050	none	450 N_2	20.0
17	2.5	1050	none	450 H_2N_2	19.8
18	2.5	1050	3	350 N_2	30.1
19	2.5	1050	3	450 N_2	28.7
21	2.5	1050	3	450 H_2N_2	27.5
23	2.5	1050	100	450 N_2	21.5
24	2.5	1050	100	350 H_2N_2	21.5
25	2.5	1050	100	450 H_2N_2	25.3
27	5.0	950	none	450 H_2N_2	8.8
29	5.0	950	3	350 N_2	11.4
30	5.0	950	3	450 N_2	10.3
32	5.0	950	3	450 H_2N_2	10.2
33	5.0	950	3	410 N_2	9.4
34	5.0	950	3	450 H_2	19.4
35	5.0	950	100	350 N_2	10.3
37	5.0	950	100	350 H_2N_2	8.6
38	5.0	950	100	450 H_2N_2	8.6
39	5.0	950	100	410 N_2	9.8
40	5.0	950	100	450 H_2	34.9

contact dope came after the hydrogen anneal. This problem also plagued the next hydrogen attempt, which was the run CR-3C. In this case, the hydrogen treatment was performed by hydrogen implant. Once again, the hydrogen seemed to have little or adverse effect, which can be attributed to the traveler error. This excuse doesn't hold for the last try; CR-4. In this case, the traveller was correct, and hydrogen was implanted at the right step in the process. Unfortunately, the results were even more conclusive, and still indicate that the hydrogen treatment makes the polysilicon more resistive, see Table 7.4. In this run, a hydrogen anneal was also run, and compared with slices from the same lot that received a forming gas anneal (90% N_2, 10% H_2). Here there was a dramatic increase in the resistance of the hydrogen annealled samples relative to the forming gas devices. At this point there is no explanation why these results are in contradiction to the published results.

7.4: Application to Other Works

In this section, the general application of the developed model will be investigated. The procedure used for this study was to find reports in the literature where experimental results on similar material are presented, and to make the calculations for the data as presented. Two papers were chosen [8,15], the works of Lu et al. and Huang et al. Both of these papers describe experiments very similar to that undertaken by this study, but use much different models to examine the results. It is seen that the model of this study does quite well at fitting the data functions presented by these reports, see Figures 7.9 and 7.10. Also, the calculated parameters are presented in Table 7.5, where it is noted that the carrier density used is the value taken from the papers directly, without any adjustments. The value for the surface-to-volume ratio for the calculation was estimated based on the results of this study and the reported thermal treatments. It is noted that the data presented by both papers, and by Huang especially, is a much more severe temperature function than the data collected by this study, but the model still fits the data to with about 10% at the very worst. It should be added that the new model makes a better fit to the data of these reports than the model utilized by the authors. A final note on the results of Huang et al. is that their data functions are such extreme plots that very high values of the barrier height were necessqary to fit the data. Several of the curves result in average barriers in excess of one volt, which is much higher than any previous report in the literature. This is surely unphysical since it would require very large charge densities to maintain such a barrier, and if the situation did exist, the formulation might need to be reevaluated to make sure that this did not require additional assumptions to be made.

7.5: Hall and Current-Voltage Measurements

In this section, further experimental results obtained by this study will be presented. These include the results of the Hall Effect measurements, where it is found that the carrier density is an constant over temperature, and the current-voltage measurements, where the classical sinh function was not reproduced.

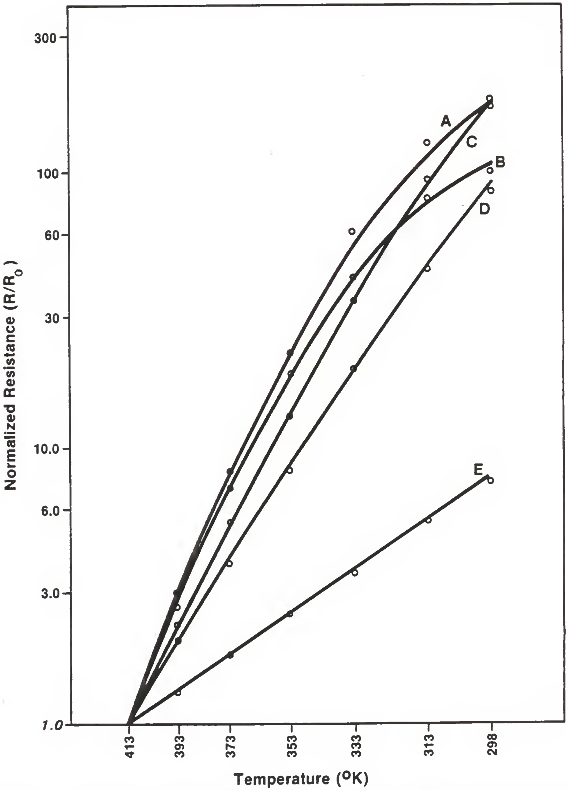


Figure 7.9: Application of the new model to the data presented by Lu et al.(8)

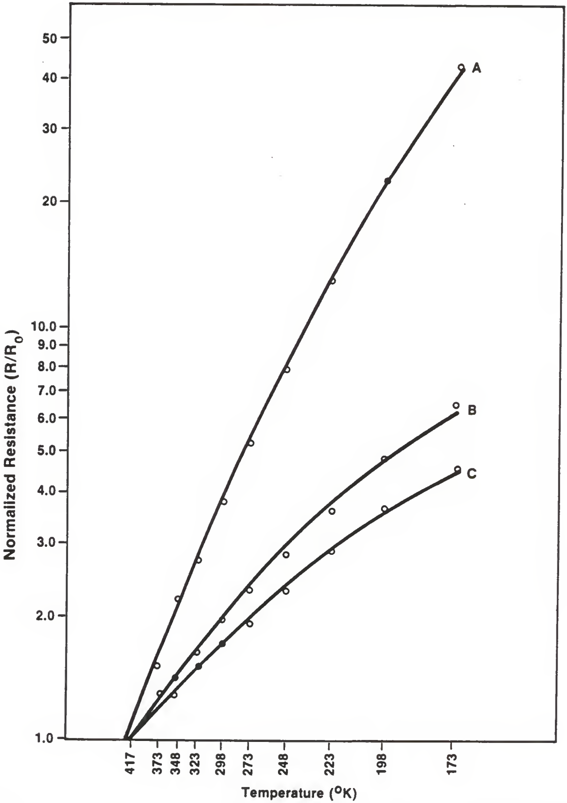


Figure 7.10: Application of the new model to data presented by Huang et al.(15)

Table 7.5

Parameters for the Data of Lu and Huang

sample	$\langle V_d \rangle$ volt	sigma volt	E_a(RT) volt	R_o	S_v 10^5 cm^{-1}
Lu A	.215	.046	.173	$4.57x10^{-3}$	3.82
Lu B	.145	.040	.113	$2.42x10^{-2}$	3.82
Lu C	.122	.036	.096	$4.10x10^{-2}$	3.82
Huang A	2.433	.240	1.310	$1.23x10^{-20}$	5.61
Huang B	2.503	.247	1.314	$6.42x10^{-21}$	5.61
Huang C	1.074	.130	.744	$4.94x10^{-11}$	5.61
Huang D	.661	.081	.532	$9.20x10^{-8}$	5.61
Huang E	.229	.0195	.221	$1.47x10^{-3}$	5.61

sample	N cm^{-3}	Nt cm^{-2}	Nt cm^{-3}	Ntot cm^{-3}
	$10^{17}cm^{-3}$	$10^{12}cm^{-2}$	$10^{17}cm^{-3}$	$10^{18}cm^{-3}$
Lu A	5.2	2.16	8.23	1.34
Lu B	8.92	2.28	8.72	1.76
Lu C	10.0	2.23	8.51	1.85
Huang A	1	2.60	14.6	1.56
Huang B	2	3.68	20.7	2.27
Huang C	10	6.20	34.8	4.48
Huang D	20	7.41	41.6	6.16
Huang E	40	6.76	37.9	7.79

Hall Effect

In this section, the results of the Hall Effect measurements will be discussed. This characterization technique allows the calculation of the values of the resistivity, the carrier density and the carrier mobility. These parameters were investigated as a function of temperature over the range of 100-400 °K. As we have seen, the function of resistivity versus temperature is central to this study and has already been discussed. The important contribution of the Hall effect measurements is the determination of the value of the carrier density in the bulk of the grains. There has been much discussion in the literature about the interpretation of Hall measurements on polysilicon [1,31], and for the case considered by this study, namely small grains, it has been shown that the Hall density is a good measurement of the concentration in the bulk of the grains [31]. This information is important for the calculation of the majority carrier census, which will add the carrier density in the grains to the calculated density at the grain boundary to get the total number of electrons available in the material. Sample Hall data as a function of temperature are shown in Figure 7.11. The important result is quite clear, that the Hall density is constant with temperature for a wide range of measurement temperature, implant dose and anneal temperature. Thus, the constant carrier density was used in the model development. The trends are quite explicit; for different anneal temperatures, the higher anneal temperature results in a higher carrier density. It is noted that the 10^{15} cm^{-2} implanted slices show carrier densities

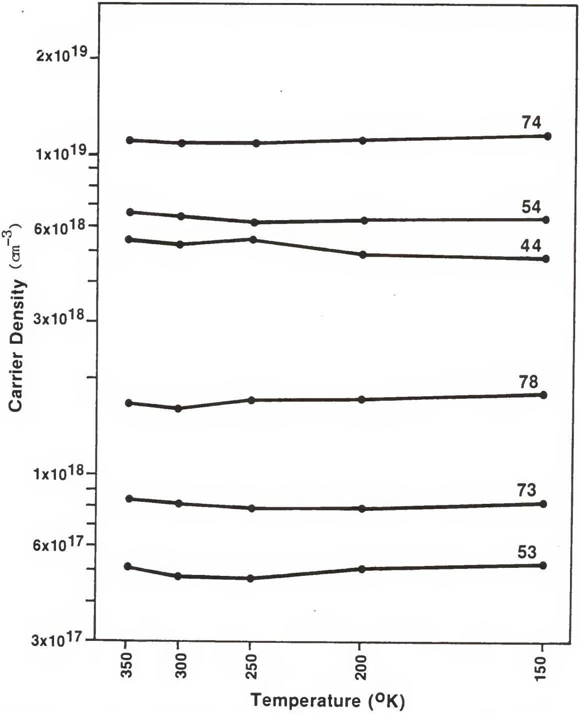


Figure 7.11: Hall Effect results of the carrier density for samples from runs CR-1 and CR-2. Notice that the carrier density is approximately constant for all devices.

Table 7.6

Hall Effect Results at Room Temperature

slice	carrier density 10^{17} cm^{-3}	mobility cm^2/volt sec	sheet resistance ohms per square
43	4.1	.045	6.7×10^6
48	4.4	.0112	2.53×10^7
53	4.8	.0072	3.61×10^7
73	8.1	2.14	7.20×10^4
78	15.6	19.0	4210
44	52	20.0	1200
49	73.1	17.1	1000
54	63.7	26.2	750
74	107	35.2	332

much less than the implant would provide in single crystal silicon, with only 25-30% of the implant dose providing carriers when the anneal is 1000 °C or less. This indicates that either dopant segregation or carrier trapping has removed a large percentage of carriers from conduction. At the higher implant dose, the percentages are much higher, in accordance with expectations of the trapping model, but too large for the classical dopant segregation model. The complete set of Hall data at room temperature are presented in the Table 7.6, and show the trends of the carrier density and mobility for the devices which were tested with this method. It is noted that the Hall measurement was not successful for all samples in this study. Those samples with implants of 10^{13} cm^{-2} or less has zero field transverse voltages much larger than the Hall voltage, and thus the carrier density could not be determined. Similar problems were encountered with an occaisonal sample of higher implant dose, and is atributed to enough nonuniformity to ruin the measurement. Also, appropriate nonmagnetic packaging is nonstandard at Harris (the standard military packages all use kovar, a magnetic material, to match the thermal expansion of the ceramic; all plastic packaging is done in Malaysia), so the later devices were not tested on this measurement. These slight problems do not seriously impact the usefulness of the measurement in this study. As for the mobilities, it is seen that the results show values in the range of 20 to 50 cm^2/volt sec. These results are well in line with similar results reported in the literature for similar material. Unfortunately, not enough different dopant densities were available to clearly show the minimum in mobility which is expected, though it is not counterindicated either. The Hall measurement is seen to contribute to an important part of this study and provides important information for the majority carrier census.

I-V measurements

Another technique which provides some information about these resistors is their current-voltage characteristics. In the model development, it is discussed that an accepted technique for this material is to characterize the "electrical effective" grain size through the use of the high voltage I-V characteristics. By a series of assumptions discussed in the modelling chapter, one can arrive at the hyperbolic sine function as the voltage dependence of current for this material [47]. In this model, the number of grains, N_g, appears in the argument of the sinh, and this is the foundation of the grain size technique. Since the grain size is very important for this study, this technique was undertaken to correlate to the other measurements. Much work later, it was decided that the technique does not perform for the devices under this study. This conclusion was reached because the values of grain size extracted were not reasonable, and did not obey necessary criteria. The problems can best be illustrated by considering a rectangular resistor, where the goal is to extract the number of grains along its length. A necessary requirement for the technique to work is that the number of grains must scale with resistor length, that is the grain size be constant for resistors of different lengths. Reports in the literature, such as Lu et al. [5] that use this technique, show data where this requirement is clearly satisfied. The work of this study, however, come to the opposite conclusion, as shown in Figure 7.12. Here are shown the high voltage I-V functions for resistors off the same die that have different lengths and widths. Also shown is the least square fit of the appropriate form to the data. It is seen that the expected sinh form does not closely fit the data and that the slope of these lines, which correspond to the extracted grain sizes, is about the same regardless of the length or width. Thus, this technique is not reported further in this study.

The alternative description of the I-V function which is utilized in the model development is the low voltage approximation. In this case, the I-V function becomes linear with the slope proportional to the resistivity of the material. In all material studied, the characteristics are linear for low voltages, although the definition of low voltage must be carefully chosen for the higher resistance devices. The resistivity calculated from I-V measurements correspond closely with the result of the van der Pauw test.

7.6: Transmission Electron Microscope Results

In this section, the results of the Transmission Electron Microscope investigation of the structure of the thin film polysilicon material will be described. The primary use of this experiment in the author's study of polysilicon is to determine the distribution of grain sizes and thus calculate the surface to volume ratio. Samples were prepared and analyzed so that the surface to volume ratio could be determined as a function of the process

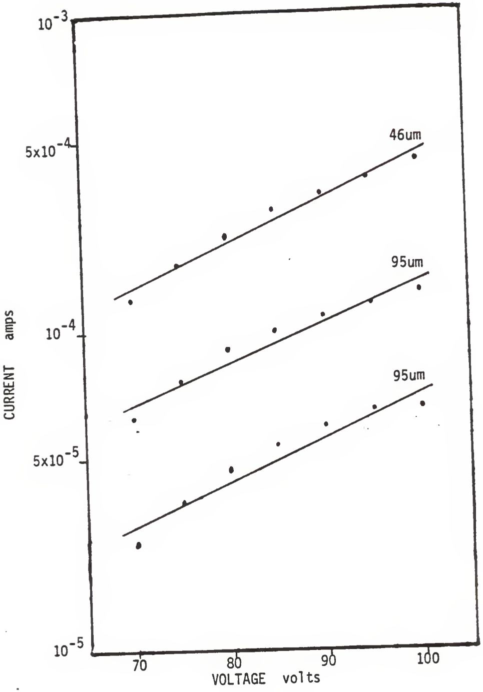


Figure 7.12: An attempt at the hyperbolic sine model, but the theory does not fit the data. These curves should have much differing slopes.

history of the polysilicon material. The most important process parameter is the anneal temperature,, with some influence of the implant dose when it is very large. This section will present the TEM images obtained, and show the results of the calculation of the surface to volume ratio. All TEM experiments were performed on the JEOL 200CX STEM.

The results of this part of the study will be presented in order of increasing anneal temperature. Thus, the first sample group to be examined is the group which received no anneal. Typical images are shown in Figure 7.13. It is noted that these and all images presented are shown at a true magnification of 100k and the scale is 1 cm equal to 100 nm. It is clearly seen in Figure 7.13 that the grains are less than 1 cm in diameter, and the approximate average size is 750 A. Although these samples received no anneal, this is not as deposited material since the process included several cycles, notably the contact predep that are at high enough temperature for some grain growth to occur. It is noted that the grains in Figure 7.13 are somewhat hard to isolate, due to the fact that the transmission nature of the image coupled with the small grain size means that several grains are stacked at each location, making the image clouded.

Next the material annealed at 900 ^{o}C is examined. It is seen in Figure 7.14 that this material is very similar to the previous case. This indicates that not much grain growth occurs at 900 ^{o}C, and this has been reported in the literature [11,42]. This material has an approximate average grain size of 800 A. This is still very

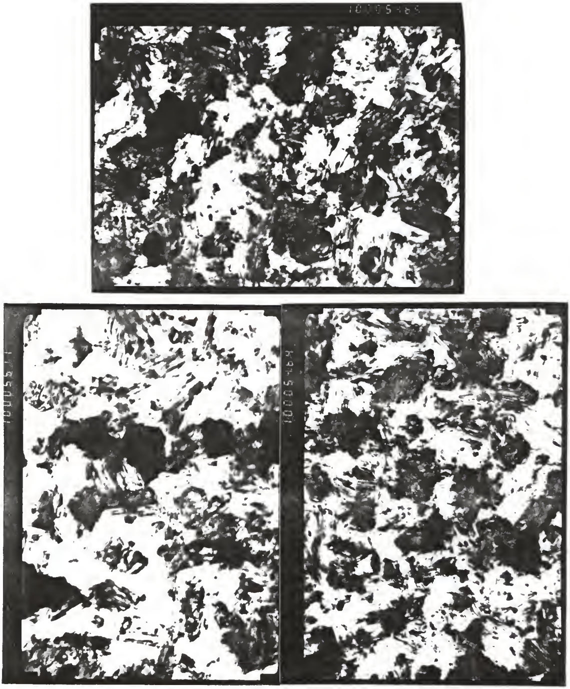


Figure 7.13:Typical TEM images from polysilicon which received no additional anneal beyond necessary process.

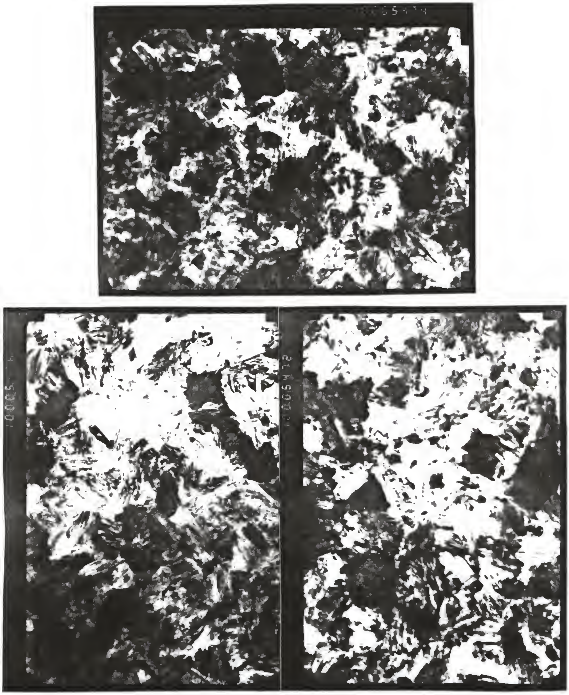


Figure 7.14: Typical TEM images from polysilicon which received an anneal of 900 °C.

small grains, and the electrical properties already discussed also show very similar results for the unannealed and 900 ^{o}C materials.

The material annealed at 1000 ^{o}C is shown in Figure 7.15. Here it is seen that the grains are slightly larger and have surpassed the 1 cm or 1000 A size on the average. The approximate average diameter is 1050 A. In these images, the grains are beginning to become more distinct due to the decreasing number of grains traversed by the electron beam as it passes through the sample. This allows more details within the grains to be seen, and with these images, some finer details such as shape contrast can be noticed.

With the next entry in the anneal sequence, 1100 ^{o}C, significantly larger grains are immediately recognised in Figure 7.16. It has been indicated in the literature that the temperature of 1050 ^{o}C is where grain growth begins in earnest [11,42]. With the growth that has occured in this material, detail is clearly becoming evident. In some images, twins and stacking faults are now observed. Also, all grains are much clearer due to the lower number of grains in the beam path. It is noted that the approximate grain size has increased to around 1550 A. Although this is still small grains on any kind of macroscopic scale, it is seen in the electrical parameters that the growth has made an important difference in the electronic properties. This material is beginning to have the kind of structure and properties that can be more easily handled for practical applications.

The final element in this anneal sequence is the 1200 ^{o}C samples. The typical images for this material are shown in Figure

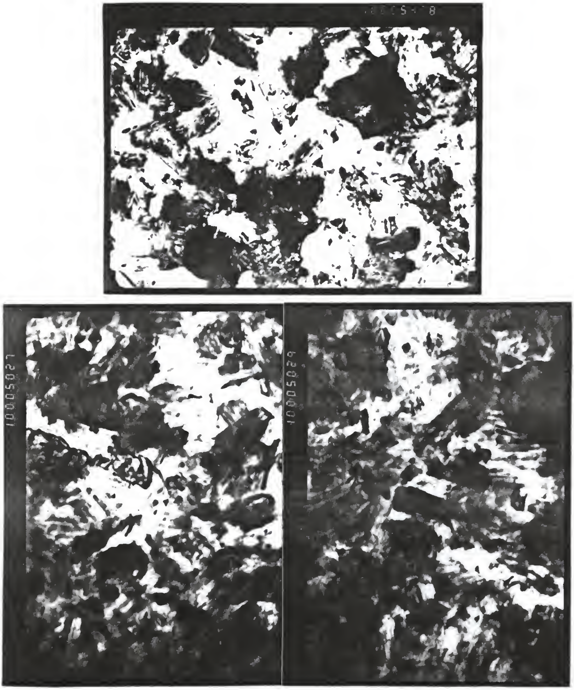


Figure 7.15: Typical TEM images from polysilicon which received an anneal at 1000 °C.

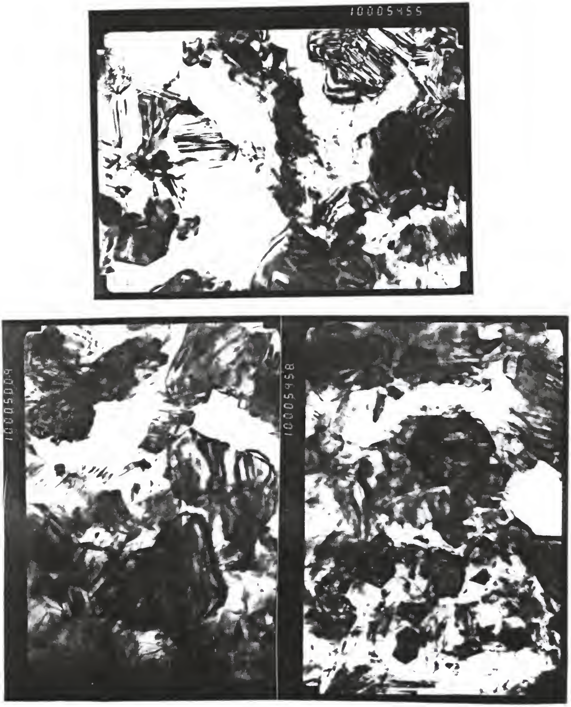


Figure 7.16: Typical TEM images from polysilicon which received an anneal at 1100 ^{o}C.

7.17. It is seen that the trends of the last entry are continued, larger grains, clearer images, more detail. The alternating light and dark bands on these grains are due to shape contrast as the diffraction conditions change with the thickness of the grains. This is seen to make some interesting images. It is also noted that some of the large grains are so clear that it appears they might be as thick as the film thickness, since no other grains are seen to overlap. The average grain size is noted to be about 1900 A for this material. Also noted is that the electrical results of this material show significantly increased variance, which could be attributed to the grains being too large, resulting in properties that could depend on whether a certain grain or grains are involved.

Table 7.7: Results of Surface-to-Volume Ratio

anneal temperature	$S_v x10^5$ cm^{-1}	$\langle L \rangle_a$ A	$\langle L \rangle_p$ A
none	5.73	743	787
900 °C	5.10	812	814
1000 °C	4.06	1032	1047
1100 °C	2.45	1520	1576
1200 °C	2.03	1802	1971

This table presents the results of the calculation of the surface to volume ratio as a function of anneal temperature. It is seen that the ratio decreases with increasing temperature, as expected due to the inverse relationship to grain size. The surface to volume ratio was determined in this study by taking the TEM images and measuring the individual grains for area and circumference, or perimeter. Thus, the values reported as surface

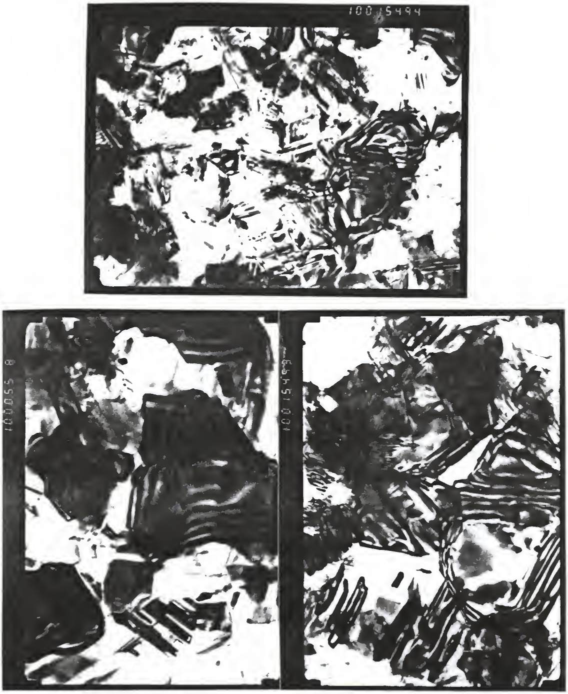


Figure 7.17: Typical TEM images from polysilicon which received an anneal at 1200 °C.

to volume ratio (three dimensions) were actually evaluated as perimeter to area ratio (two dimensions). This is not an ideal situation, but is the best that can be expected given the two dimensional nature of the photographs obtained from the TEM. It will assumed that the numbers are valid. The last two columns of the table are the average grain size which is determined from the area average and the perimeter average, assuming cubic grains. These numbers are only estimates of an average, and are meant to be evidence that the procedure outlined for the use of the surface to volume ratio is important. The idea behind using the surface to volume ratio was that the small grains in the material contributed more surface area than the larger grains, and thus care must be taken to analyze the material so that the important property, the boundary area is determined correctly. The two columns in the table show that the cubic approximation yields a larger estimate of the grain size when the perimeter average is used than when the area average is used. Thus, more perimeter relative to area exists, and this is exactly the prediction. Although the magnitude of the differene varies, it is a clear trend. These values are the basis for the approximate grain sizes noted above, which were intended to be an average of the two approximate grain sizes.

Another factor in determining the grain size in polysilicon material is the implant dose. The amount of impurities at the grain boundaries can affect the grain growth process, which also occurs at the grain boundaries. Images for polysilicon of various implant doses which has been annealed at 1100 °C are shown in Figure 7.18.

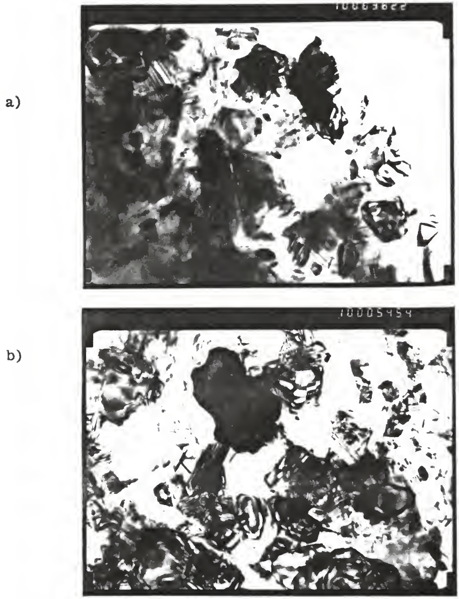
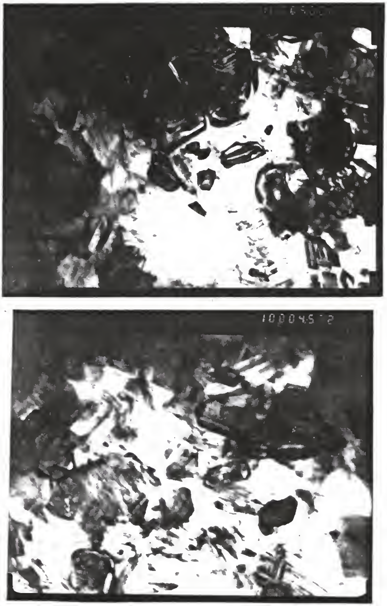


Figure 7.18: TEM images showing the implant sequence on samples annealed at 1100 °C; a) implant dose of 10^{12} cm^{-2}, b) implant dose of 10^{13} cm^{-2}.


c)

d)

Figure 7.18: TEM images showing the implant sequence for samples annealed at 1100 ^{o}C; c) implant dose of 10^{14} cm^{-2}, d) implant dose of 10^{15} cm^{-2}.

e)

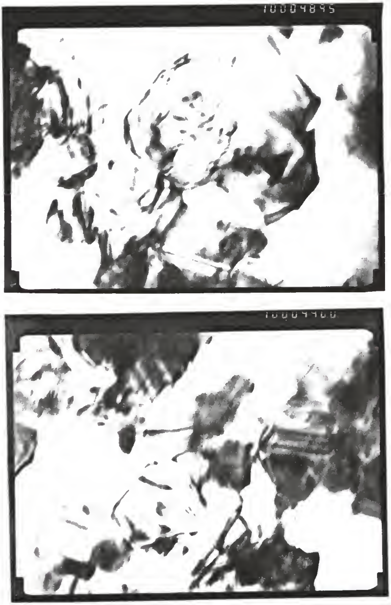


Figure 7.18: TEM images showing the implant sequence on samples annealed at 1100 ^{o}C; e) both were implanted at 10^{16}cm^{-2}.

Here it is seen that the lower doses, 10^{12} to 10^{14} cm^{-2} do not have much effect on the grain size. The heaviest dose, 10^{16} cm^{-2}, however, is seen to have a substantial effect, and increases the size of the grains. This trend has been reported in the literature [42]. The heavy implant samples have an approximate grain size of 2100 A, or an increase in size of about 30%. This effect is present at all anneal temperature, as seen in Figure 7.19 where the heavy implant samples annealed at 1000 °C are shown, and have much larger grains than the less implanted samples shown in Figure 7.15.

A final presentation of the TEM results is Figure 7.20, which shows the grain area distribution functions for two of the anneal temperatures. It is seen that the grain sizes follow approximately a Gaussian distribution, and that the higher temperature anneal has the same trend with about three times larger grains. These distribution functions closely reflect a similar distribution reported in the literature [5].

In summary, the TEM is very useful for obtaining the microstructure information in thinfilm pollysilicon. Images for the various anneal temperatures have been shown, as well as the implant effect, the surface to volume ratios and the grain area distribution functions. The predicted effect of accurately incorporating the small grains in the material is clearly shown.

7.7: Capacitance Effects

Additional experiments were undertaken to determine some of the capacitance properties of the polysilicon material. These experiments were variously successful. This chapter will explain

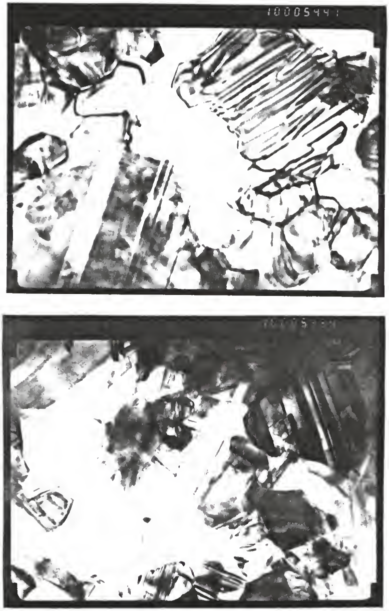
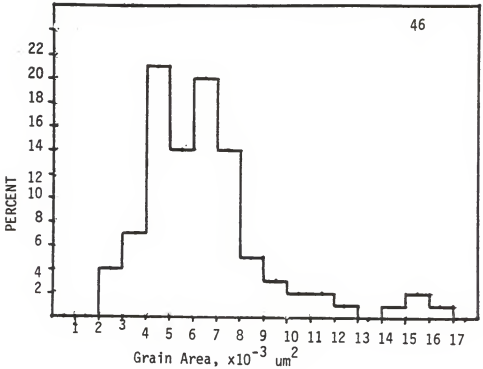


Figure 7.19: TEM images for heavy implant samples annealed at 1000°C.



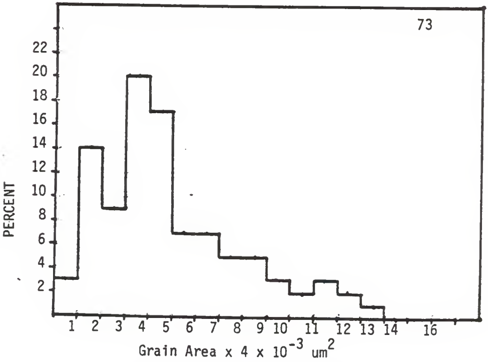


Figure 7.20: Distribution functions of grain area as determined by TEM for two slices from this study.

the experiments undertaken and the results obtained. Once again, all devices were fabricated at Harris Semiconductor. The experiments will be described in conjunction with the description of the test device. The devices studied were thin-film parallel plate MOS capacitors, thin-film rectangular resistors, and the substrate of complete integrated circuits. The experiments lead to some information concerning the grain boundary capacitance in polysilicon and show how this can affect performance of polysilicon circuit elements and substrate materials.

The first experiment undertaken was the fabrication of thin-film polysilicon capacitors. This occurred along with fabrication of the thin-film resistors of runs CR-1 and CR-2. These runs were split so that an identical group of wafers were processed into capacitors and resistors so that the material characteristics would match. The polysilicon material was used as the semiconductor side of MOS capacitors of various sizes. These capacitors had 1000A of LPCVD oxide as the gate dielectric. The upper electrode was the same metal as used for interconnect on the resistor splits, namely electron beam evaporated aluminum. The processing followed the same flow as the resistor runs, with variables of anneal temperature and implant dose matrixed over extended range. The mask set which was used was 1410. These capacitors turned out to be marginally useful, as the dielectric was not good enough to provide useful data. It was found that the combination of high sheet resistance in the polysilicon and some conductance through the oxide caused the classical MOS capacitor characteristics to be obscured. Most of the devices tested showed strong leakage through the oxide. Many of those which originally appeared intact were seen to breakdown during the measurement. This initial measurement technique consisted of standard C-V testing with the PAR 410 in the physical electronics lab. It is noted that at least five die (often many more) were tested from each surviving wafer (from 80 wafer start) with less than 25 good capacitors being located. It was found that the most likely process to produce a good capacitor was the most heavy implant dose followed by the highest temperature anneal. These steps were found to produce a capacitor with very classical paraollel plate characteristics, i.e. no MOS characteristics observed. From the constant parallel plate capacitance, the only parameter to be calculated is the oxide thickness, which was calculated to be within 10% of the process specification. No other material characteristics were determined from this experiment. It is now expected that the combination of resistance and capacitance in the thin-film MOS layer prevented observation of classical characteristics in these devices.

The next set of measurements to be made on the capacitance of polysilicon involved measureing the substrate parasitics on completely fabricated integrated circuits. In this case, the characteristics of polysilicon enter because the substrate is CVD polysilicon grown "on the back" through the dielectric isolation (DI) process. Many circuits at Harris use this technology to achieve higher performance. One of the advantages of DI material is that the substrate parasitics are much less than a junction isoloated circuit would have, and thus higher performance is possible. This part of the study was done to better characterize the frequency characteristics of the substrate parasitics. This study included measurements of the substrate capacitance and resistance as a function of frequency, from a circuit element. This measurement was repeated over the same circuit fabricated on substrate material of differing resistance. It is found that these measurements reveal some interesting properties concerning the resistance and capacitance functions of frequency. The measurements were from the circuit element to substrate, series resistance and capacitance, measured as a function of frequency with the HP 4275 LCR meter. The results show a sharply declining function for both resistance and capacitance. The explanation involves both the material characteristic of the polysilicon, and the effects of the other parts of the structure. First, the low frequency capacitance corresponded closely with the expected capacitance of the insulating dielectric. The parallel plate nature of this capacitance indicates that it should be independent of frequency. The low frequency resistance is also understood as the series resistance of the island material and the substrate material. In some cases the polysilicon substrate was undoped, resulting in very high resistance. The devices could not be measured at low frequencies, but had rapidly falling resistance terms for the higher frequencies. The doped substrates had low frequency resistance corresponding to the doped conductance properties, with a break frequency and rapidly decling resistance as frequency is increased. Both the declines of the capacitance and the resistance are explained by including the

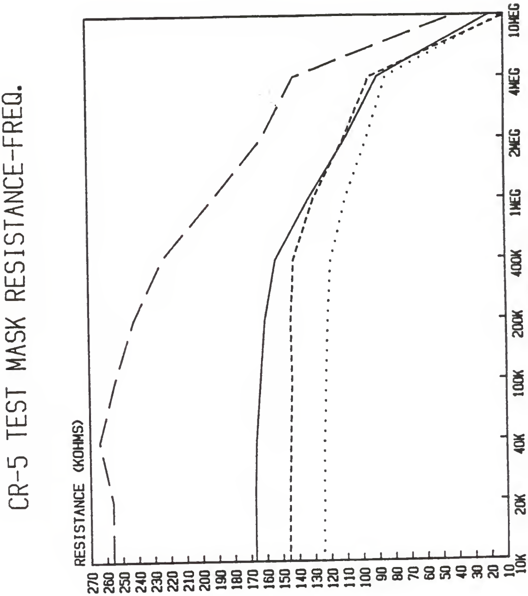


Figure 7.21: The resistance to substrate versus frequency for undoped polysilicon capacitors.

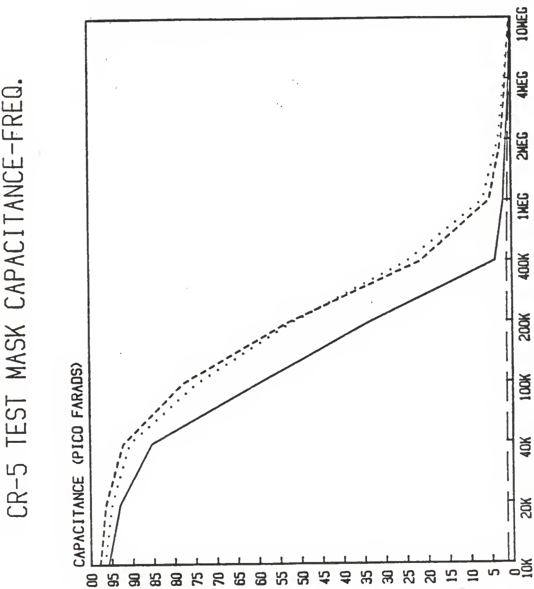


Figure 7.22: The capacitance to substrate versus frequency for undoped polysilicon capacitors.

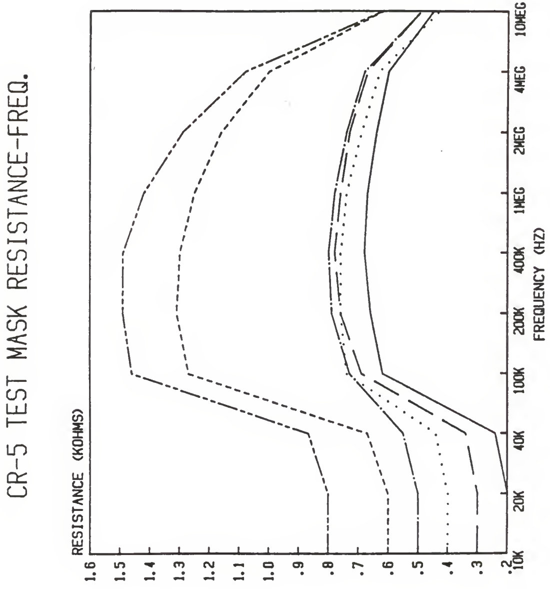


Figure 7.23: The resistance to substrate versus frequency for doped polysilicon capacitors.

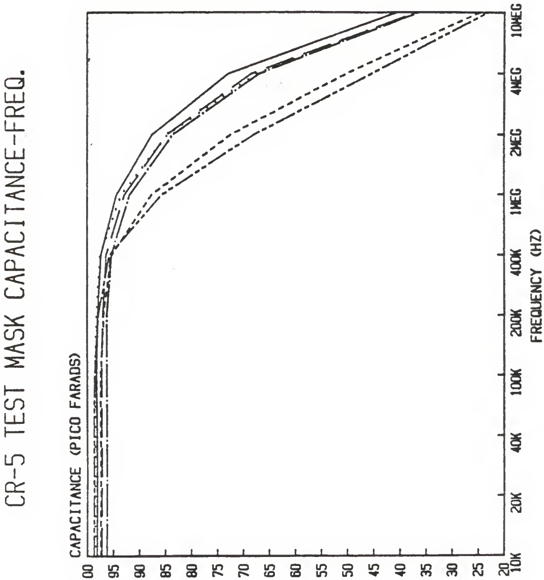
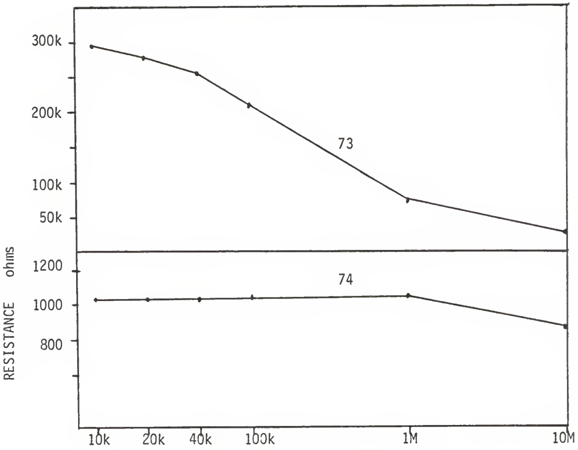


Figure 7.24: The capacitance to substrate versus frequency for doped polysilicon capacitors.

grain boundary capacitance of the polysilicon. This capacitance appears in parallel to the grain boundary resistance, at each boundary. The capacitance comes about from the separation of charge created by the grain boundary trapping of majority carriers. Since most of the resistance of the polysilicon also appears at the grain boundary, these two are in parallel and can potentially shunt each other. The observed phenemonon suggests that the grain boundary capacitor has less impedance as the frequency is increased, and a point is reached where the capacitor shunts out the grain boundary resistance and becomes the dominant element in the polysilicon impedance. This happens at the break frequency in the doped substrate cases and at low freqencies in the cases where the substrate is very high resistance and thus sensistive to being shorted out. This capacitor shunting of the polysilicon resistance has strong effect on the measured capacitance also since the insulator capacitor now appears in series with the polysilicon capacitance. This explains the rapid decline of the measured capacitane, and its observed break frequency in the doped samples. Finally, it is noted that the rapid decline of resistance and capacitance was observed to have a degrading effect on the circuit function. Thus, it is recommended that high performance circuits be fabricated on doped polysilicon substrates. This will present slightly higher capacitance to substrate, with the benefit of avoiding the unwanted shunting effects.

A final series of measurements were performed to further investigate this capacitance effect on polysilicon. In this case, the IC resistors used in the rest of the study were measured for



FREQUENCY Hertz

Figure 7.25: Resistance versus frequency for two samples from run CR-1. Notice the difference one order of magnitude of implant makes.

resistance and capacitance as a function fo frequency using the HP 4275 LCR meter. It was found that high resistance material had the same declining function characteristic as the substrate material just discussed. Furthermore, the doped material had a break frequency characteristic very similar to the doped substrate material. In this experiment, it is found that the maximum frequency of resistance varied with the doping and other process variables. The effects of the capacitance are insignificant as long as the resistance of the material is less than the impedance of the capacitor. Otherwise, the capacitor dominamtes the impedance. It is noted that the polysilicon material would have to be about 1Mohm per square before this would present a problem for typical circuits speeds.

In summary, some experiments were conducted to investigate the frequency and capacitance nature of the polysilicon material. These experiments were variously successful. The attempts at thin-film MOS capacitors was unsuccessful because of the lack of oxide integrity. The measurements of the DI substrate and the frequency characteristics of the IC resistors showed that the capacitance of the grain boundaries cannot be neglected, and can have significant impact under certain circumstances. It is seen that high resistance polysilicon has the most problems in this area. The experiments suggest that this might be a fertile area for further study.

This chapter presented the experimental results of this study. It has been seen that measurements of resistivity versus temperature, Hall effect versus temperature, and transmission electron microscope were the primary techniques of this research. In addition, other measurements and analyses were performed with the general result thatthe model developed in Chapter IV is seen to accurately model the experimental results, and that the theoretical discussions of this presentation are supported by experimental evidence.

CHAPTER VIII

SUMMARY AND COMMENTS

This study investigated the properties of polysilicon with the explicit emphasis on providing a practical explanation for the electrical characteristics observed in this material. The primary characteristic which was observed which had not been previously characterized was the obvious nonuniformity, and this became the focus of this investigation. The model developed by this work incorporates a technique for mathematically handling the variation of parameters throughout the material.

The mathematic basis for the modeling of this study is the use of distribution functions. It is shown that the distribution function can be used to provide an accurate formulation for achieving an evaluation of polysilicon without needing to make some of the limiting assumptions utilized in the past. The explicit parameters which have been developed into distribution functions by this study are the grain size and the grain boundary barrier heights, and both of these have been shown to be properly behaving in the new model. An outcome of this procedure is that the resistivity function of temperature can be explained using only the thermionic emission mechanism.

Some further investigations of the parameters of polysilicon were performed with the following results. The carrier density was studied and the importance of properly using the carrier density or the doping density was indicated. An experimental study of the carrier density shows that it is a constant over temperature for the material studied in this work. Also, the effects of a profile in the dopant density near a grain boundary was studied, with the result that this analysis indicated an interrelationship between the carrier trapping and dopant segregation models which had not previously been reported.

The study included a significant experimental portion. In total, more than 300 wafers were processed for this study by Harris Semiconductor. Experiments were performed which clearly show the developed model at work over the entire range of practical polysilicon process variables. The attempts at studying the hydrogenation and capacitance effects in polysilicon were somewhat dissappointing.

In summary, this study developed a new theoretical model for the resisitivity function of temperature for thinfilm polysilicon material. The model is shown to be valid for the measurements of this and other studies. It is believed that the new description is a useful contribution to understanding the practical aspects of conduction in this material.

APPENDIX A

BASIC PROGRAM FOR DETERMINATION OF BARRIER STATISTICS

On the following pages is a printout of the program used to determine the parameters of the model for resistivity. The program uses the data of sheet resistance versus temperature as input and calculates the necessary parameters of average barrier height and the standard deviation of barrier heights. It is seen to be a simple least square regression.

```
5 HOME
10 PRINT "n/th order regression"
20 DIM A(13),R(7,8),T(8)
22 DIM TEMP(9)
23 KB = 8.614E-05
24 TEMP(1)=225:TEMP(2)=250:TEMP(3)=275:TEMP(4)=300:TEMP(5)=325
25 TEMP(6)=350:TEMP(7)=375:TEMP(8)=400:TEMP(9)=425
30 PRINT
40 PRINT "degree of equation"
50 INPUT D
60 PRINT "number of known points"
70 INPUT N
80 A(1) = N
90 FOR I=1 TO N
92 READ RHO
95 X = 1/(KB*TEMP(I))
97 Y = LOG (RHO/TEMP(I)) + 1.5*LOG(X)
100 PRINT "x,y of point #";I;"  = ";X;Y
120 FOR J = 2 TO 2*D+1
130 A(J) = A(J) + X^(J-1)
140 NEXT J
150 FOR K = 1 TO D+1
160 R(K,D+2)= T(K) + Y*X^(K-1)
170 T(K) = T(K) + Y*X^(K-1)
180 NEXT K
190 T(D+2) = T(D+2) + Y^2
200 NEXT I
210 FOR J = 1 TO D+1
220 FOR K=1 TO D+1
230 R(J,K)= A(J+K-1)
240 NEXT K
250 NEXT J
260 FOR J=1 TO D+1
270 FOR K = J TO D+1
280 IF R(K,J) <>0 THEN 320
290 NEXT K
300 PRINT "no unique lolution"
310 GOTO 790
320 FOR I=1 TO D+2
330 S = R(J,I)
340 R(J,I) = R(K,I)
350 R(K,I)= S
360 NEXT I
370 Z= 1/R(J,J)
380 FOR I=1 TO D+2
390 R(J,I) = Z*R(J,I)
400 NEXT I
410 FOR K=1 TO D+1
420 IF K=J THEN 470
430 Z = -R(K,J)
440 FOR I=1 TO D+2
450 R(K,I) = R(K,I) + Z * R(J,I)
460 NEXT I
470 NEXT K
480 NEXT J
```

```
485 PRINT
490 PRINT "               constant=";
496 PRINT R(1,D+2)
500 FOR J=1 TO D
510 PRINT J;"degree coeficient=";
511 PRINT R(J+1,D+2)
520 NEXT J
530 PRINT
540 P=0
550 FOR J=2 TO D+1
560 P=P+R(J,D+2)*(T(J)-A(J)*T(1)/N)
570 NEXT J
580 Q= T(D+2)-T(1)^2/N
590 Z=Q-P
600 I=N-D-1
620 PRINT
630 J=P/Q
640 PRINT "coefficient of ";
641 PRINT "determination"
645 PRINT "(r^2) =";J
650 PRINT "correlation coefficient =";
651 PRINT SQR(J)
660 PRINT "standard error estimate =";
661 ZZ=ABS(Z/I)
662 PRINT SQR(ZZ)
670 PRINT
680 PRINT "interpolation: ";
681 PRINT "(enter 0 to end)"
690 P=R(1,D+2)
700 PRINT "x=";
710 INPUT X
720 IF X=0 THEN 5000
730 FOR J=1 TO D
740 P=P+R(J+1,D+2)*X^J
750 NEXT J
760 PRINT "y=";P
770 PRINT
780 GOTO 690
1000 DATA 1327,1201,1092,1014,947,888,840,806,777
5000 END
```

APPENDIX B

BASIC PROGRAM FOR CALCULATION OF AVERAGING INTEGRALS

On the following pages is a printout of the program developed to calculate the averages by integration of the distribution functions. This program is explicitly setup to do the Gaussian function used by this study for the barrier heights, but could handle any other distribution function with modification. It is seen that this program does a modified Simpson rule evaluation of the integral.

```
100 HOME
105 PRINT "       "
107 PRINT:PRINT:PRINT
110 PRINT "   welcome to     "
111 PRINT:PRINT "    integral evaluation    "
112 PRINT:PRINT "    by means of the    "
115 PRINT:PRINT "    modified simpson method   "
117 PRINT:PRINT "    by WAK, 2-27-84   "
120 PRINT:PRINT:PRINT:PRINT
130 PRINT
140 INPUT "enter integration limits: lower,upper ";A,B
145 PRINT:PRINT
150 INPUT "enter doping density ";ND
155 PRINT:PRINT
160 PRINT:PRINT "enter g.b. dist. parameters  "
170 INPUT "(average barrier, standard deviation)";VD,S2
180 PRINT:PRINT
190 E=1
200 M = (A+B)/2
205 H1 = (B-A)/40
210 GOSUB 390
218 REM ==EVALUATE PRINCIPAL TERMS OF DEFINITE INTEGRAL==
225 INPUT "enter number of points";N
240 S = 0
243 X = A
247 H = (B-A)/N
248 PRINT "step size is ";H
249 IF S2 < H THEN PRINT "warning: step size < stand. dev."
250 FOR I=1 TO N/2
260 GOSUB 370
265 S = S + F
270 X = X + H
273 GOSUB 370
277 S = S + 4 * F
280 X = X + H
283 GOSUB 370
287 S = S + F
290 NEXT I
300 PRINT:PRINT:PRINT
310 PRINT "integration result:  ";S*H/3
315 PRINT "this is the average charge density per unit area"
320 PRINT:PRINT
330 PRINT "change number of points?"
335 PRINT "(1 = yes, 0 = no) ";
340 INPUT W
350 IF W=1 THEN 190
360 GOTO 470
368 REM==SUBROUTINE WHICH DEFINES USER FUNCTION==
370 ND2 = SQR(ND) : X1 = X-VD: X3 = X1^2
371 CON = (2893.88)*ND2*SQR(X)/S2
372 S3= S2^2: X2 = -(X3/S3)/2
375 F = CON * EXP(X2)
380 RETURN
388 REM==SUBROUTINE TO EVALUATE ERROR==
390 D=0
```

```
400 X=M-2*H1
403 GOSUB 370
407 D = D + F
410 X = M - H1
413 GOSUB 370
417 D = D - 4 * F
420 X = M
423 GOSUB 370
427 D = D + 6 * F
430 X = M + H1
433 GOSUB 370
437 D = D - 4 * F
440 X = M + 2 * H1
443 GOSUB 370
447 D = D + F
450 D = ABS (D) /H1^4
460 RETURN
470 END
```

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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